User Manual

MIC-3332

3U CompactPCI 6th Generation

Intel® Core™ i7 Processor Blade, ECC optional

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Enabling an Intelligent Planet

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Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

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1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.

2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.

3. If your product is diagnosed as defective, obtain an RMA (return merchandize authorization) number from your dealer. This allows us to process your return more quickly.

4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.

5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables.

FCC Class A

Note: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FM

This equipment has passed the FM certification. According to the National Fire Protection Association, work sites are classified into different classes, divisions and groups, based on hazard considerations. This equipment is compliant with the specifications of Class I, Division 2, Groups A, B, C and D indoor hazards.

Technical Support and Assistance

1. Visit the Advantech website at http://support.advantech.com where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   – Product name and serial number
   – Description of your peripheral attachments
   – Description of your software (operating system, version, application software, etc.)
   – A complete description of the problem
   – The exact wording of any error messages

Warnings, Cautions and Notes

Warning! *Warnings indicate conditions, which if not observed, can cause personal injury!*

Caution! *Cautions are included to help you avoid damaging hardware or losing data. e.g.*

There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.

Note! *Notes provide optional additional information.*

Document Feedback

To assist us in making improvements to this manual, we would welcome comments and constructive criticism. Please send all such - in writing to: support@advantech.com

Packing List

Before setting up the system, check that the items listed below are included and in good condition. If any item is not accord with the table, please contact your dealer immediately.

- MIC-3332 all-in-one single board computer (CPU heatsink and PCH heatsink included) x1
- Daughter board for SATA HDD x1(Assembled)
- HDD tray and screws package x 1
- Solder-side cover (Assembled) x1
- Warranty certificate document x1
- Safety Warnings: CE, FCC class A

If any of these items are missing or damaged, contact your distributor or sales representative immediately.

Safety Instructions

1. Read these safety instructions carefully.
2. Keep this User Manual for later reference.
3. Disconnect this equipment from any AC outlet before cleaning. Use a damp cloth. Do not use liquid or spray detergents for cleaning.
4. For plug-in equipment, the power outlet socket must be located near the equipment and must be easily accessible.
5. Keep this equipment away from humidity.
6. Put this equipment on a reliable surface during installation. Dropping it or letting it fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. DO NOT COVER THE OPENINGS.
8. Make sure the voltage of the power source is correct before connecting the equipment to the power outlet.
9. Position the power cord so that people cannot step on it. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage by transient overvoltage.
12. Never pour any liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If one of the following situations arises, get the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated into the equipment.
    - The equipment has been exposed to moisture.
    - The equipment does not work well, or you cannot get it to work according to the user's manual.
    - The equipment has been dropped and damaged.
    - The equipment has obvious signs of breakage.
15. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20° C (-4° F) OR ABOVE 60° C (140° F). THIS COULD DAMAGE THE EQUIPMENT. THE EQUIPMENT SHOULD BE IN A CONTROLLED ENVIRONMENT.
16. CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED. REPLACE ONLY WITH THE SAME OR EQUIVALENT TYPE RECOMMENDED BY THE MANUFACTURER, DISCARD USED BATTERIES ACCORDING TO THE MANUFACTURER'S INSTRUCTIONS.

The sound pressure level at the operator's position according to IEC 704-1:1982 is no more than 70 dB (A).

DISCLAIMER: This set of instructions is given according to IEC 704-1. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precaution - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

■ To avoid electrical shock, always disconnect the power from your PC chassis before you work on it. Don't touch any components on the CPU card or other cards while the PC is on.

■ Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a card may damage sensitive electronic components.

We Appreciate Your Input

Please let us know of any aspect of this product, including the manual, which could use improvement or correction. We appreciate your valuable input in helping make our products better.

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Chapter 1

Hardware Configuration

This chapter describes how to configure MIC-3332 hardware.

1.1 Introduction

MIC-3332 series are 3U CompactPCI single board computers with 6th Gen Intel® Quad Core™ i7/Xeon®E3 processors and CM236 chipset. It supports single-channel memory with ECC optional, up to 16 GB on board DDR4 of 2133MHz speed. There are various types of storage on the XTM board: including a 2.5" SATA connector, a Cfast socket, and an additional Micro-SD slot on the XTM-2 board. MIC-3332 is available in single and dual slot width form factors, to offer various I/O functionality by XTM(8HP) and rear I/O extensions. Front panel I/O on the single slot (4HP) provides 1x VGA port, 2 x USB 3.0 ports, and 2 x RJ45 GbE ports. Front Panel I/O on the 8HP XTM layer have multiple options; 8HP XTM-1 board provides 1x RJ45 COM port, 1 x HDMI display port, 1 x USB 3.0 port, 2 x GbE LAN ports by M12 X-coding or RJ45 connectors; 8HP XTM-2 Board provides 4 x GbE LAN ports by M12 X-coding or RJ45 connectors.

MIC-3332 provides an ideal solution for transportation, railway, and factory Automation applications. With its robust board layout and thermal efficiency, it meets and exceeds EN50155 and EN50121-4 standards.

MIC-3332 series can be installed in a standard CompactPCI system slot, designed to meet harsh environments, and is ideally suitable for data centers, telecom, military, defense systems, and many other vertical segment applications. It is compliant with PICMG 2.0 Rev. 3.0 / PICMG 2.1/ PICMG 2.3 Rev.1.0, and supports 32-bit / 33 MHz PCI bus at +3.3 V or +5 V VIO.

Ordering Information:

Single board	Front Panel								Main On board Features							
	4HP			8HP XTM					4HP		8HP XTM (Conn./Socket/Pin head)				Others	
	LAN (RJ45)	USB 3.0	VGA	LAN (M12)	LAN (RJ45)	COM	HDMI	USB 3.0	CPU	Memory	SATA Conn.	Cfast Socket	Micro-SD Socket	COM-Pin head	Slot Width	PlusIO
MIC-3332C1-D1E	2	2	1	-	4	-	-	-	i7-6822 EQ	8GB	1	1	1	-	2	No
MIC-3332D1-D1E	2	2	1	4	-	-	-	-	i7-6820 EQ	16GB	1	1	1	-	2	No
MIC-3332C4-D2E	2	2	1	-	2	1	1	1	i7-6822 EQ	8GB	1	1	-	1	2	No
MIC-3332C5-D2E	2	2	1	2	-	1	1	1	i7-6822 EQ	16GB	1	1	-	1	2	No

1.2 Specifications

1.2.1 CompactPCI Bridge

The MIC-3332 uses a Pericom PI7C9X110 universal bridge as a gateway to an intelligent subsystem. When configured as a system controller, the bridge acts as a standard transparent PCI Express to PCI/PCI-X Bridge. As a peripheral controller it allows the local MIC-3332 processor to configure and control the onboard local subsystem independently from the CompactPCI bus host processor. When the MIC-3332 is in drone mode, the Pericom PI7C9X110 is electrically isolated from the CompactPCI bus, it receives power from the backplane, and supports rear I/O only. The Pericom PI7C9X110 PCI Bridge offers the following features:

- PCI Interface
  - Full compliance with the PCI local bus specification, revision 3.0
  - Supports 3.3V PCI signaling with 5V I/O tolerance
- Supports transparent mode operations.
- Supports forward bridging
- 32-bit, 33MHz asynchronous operation
- Provides two-level arbitration support for 7 PCI bus masters
- 16-bit address decode for VGA
- Usable in CompactPCI system slot

Please consult the Pericom PI7C9X110 datasheet for details.

1.2.2 Processor

The MIC-3332 supports the Intel® 6th generation Core™i7 or Xeon® E3 Skylake processor family with clock frequencies up to 2.8 GHz and a Direct Media Interface (DMI) up to 8GT/s. Please contact local sales for Xeon/Corei3/i5/Celeron processor configurations more information.

Table 1.1: Processor Type									
Intel CPU Model Number	CPU Architecture	#Cores	#Threads	Freq.	Cache	DMI	CPU TDP	Package	Required Airflow
I7-6822EQ	Skylake (14nm)	4	8	2.0GHz	8MB	8GT/s	25W	FCBGA	30 CFM
I7-6820EQ	Skylake (14nm)	4	8	2.8GHz	8MB	8GT/s	45W	FCBGA	30 CFM
XEON E3-1505M v5	Skylake (14nm)	4	8	2.8GHz	8MB	8GT/s	45W	FCBGA	30 CFM
XEON E3-1505L v5	Skylake (14nm)	4	8	2.0GHz	8MB	8GT/s	25W	FCBGA	30 CFM

> *Note!*
>
> *Because power consumption and thermal restrictions, specifications vary between different CompactPCI systems, please double check these items before installing a higher speed CPU not listed in the table above.*

1.2.3 Chipset

The mobile Intel® CM236 chipset provides excellent flexibility for developers of embedded applications by offering improved graphics and increased I/O bandwidth over previous Intel chipsets, which offers up to 8 GT/s for fast access to peripheral devices. It delivers outstanding system performance through high bandwidth interfaces such as PCI Express Gen III, Serial ATA Gen III and Hi-Speed USB 2.0 and USB 3.0.

1.2.4 Memory

MIC-3332 has up to 16GB onboard soldered DDR4 memory, and ECC support is in Xeon processor series. Default SKUs are 8GB and 16GB on board, you can check the ordering information for the difference, or you can contact your local salesperson for more information.

> **Note!** *ECC support is optional. Please contact your local sales.*

1.2.5 Ethernet

MIC-3332 is equipped with several high-performance PCI-Express based network interface controllers which provide full IEEE802.3 compliant 10/100/1000Base-TX Ethernet interfaces. There are 2 x RJ45 GbE LAN ports on the front 4HP panel, 2 x RJ45 or 2 x M12 GbE LAN ports on front 8HP XTM-1 panel; 4 x RJ45 or 4 x M12 GbE LAN ports on the front 8HP XTM-2 panel, and another two RTM J2, You can choose RJ-45 or X-code M12 Ethernet ports based on your requirements. For details contact with your local salesperson for more information.

- Front I/O (RJ45 or M12)
- Rear I/O (Rear Transition Module)

1.2.6 Storage Interface

MIC-3332 provides up to 5 SATA III interface. Two SATA interfaces are routed to the front XTM board with 2.5" SATA connector and CFast socket; for Plus IO SKU, there are 3 x SATA available for PICMG, for Non Plus IO SKU, there are 2 x SATA available for RTM. Advantech rear board MIC-3332R1-S1E with 2 x SATA 2.0 interface with M.2 B key connector (22 x 42mm) is compatible and available, Please contact a sales representative for more details.

1.2.7 Serial ports

One RJ-45 COM1 port (RS-232/422/485) is provided on the front panel of MIC-3332. Another COM pin header with RS-232/422/485 is provided on the MIC-3332 8HP XTM-1 board. If you have problems with a serial device, be sure to check pin assignments in appendix A pin assignments. The IRQ and address range for these ports are fixed. If disabled port or parameter modification is required, please refer to Chapter 2.

1.2.8 USB Ports

MIC-3332 provides two or three USB 3.0 type A ports on the front panel and up to two USB2.0 interface for CPCI Conn via J2. The MIC-3332 USB interface complies with USB Specification R2.0 and R3.0, and is fuse protected. Please contact a sales representative for more details.

1.2.9 Watchdog Timer

An onboard watchdog timer provides system reset capabilities via software control. The programmable time interval is from 1 to 255 seconds.

1.2.10 BIOS

BIOS is a dual 16MB SPI flash containing a specific AMI BIOS FW with fail-over mechanism to meet industrial and embedded system requirements.

1.2.11 I/O Connectivity

For MIC-3332, the front panel I/O on the single slot (4HP) provides 2 x RJ45 GbE ports, 1 x VGA port and 2 x USB3.0 ports. Front Panel I/O on the 8HP XTM layer has multiple options: 8HP XTM-1 board provides 1 x RJ45 COM port, 1 x HDMI display port, 1 x USB 3.0 port, 2 x GbE LAN ports by M12 X-coding or RJ45 connectors; 8HP XTM-2 Board provides 4 x GbE LAN ports by M12 X-coding or RJ45 connectors. There are various types of storage on 8HP XTM Board: 1 x 2.5" SATA connector, 1 x CFast socket, and an additional Micro-SD socket on the 8HP XTM-2 Board.

It can also offer various I/O connectivity by Rear IO extensions and CompactPCI PlusIO.

RTM Connector	Connector Type	Reserved interface
J2	HM	■ One VGA ■ Two PCIe x1 ■ Two LAN ■ Two SATA 2.0 ■ Two USB 2.0
J2	UHM	■ Four PCIe x 1 ■ Two LAN ■ Four USB 2.0 ■ Three SATA III

1.2.12 Optional Rear I/O Modules

The MIC-3332R1-S1E is the optional RTM (also known as rear I/O module) for the MIC-3332. It offers a wide variety of I/O features, such as two RJ45 LAN ports, one VGA port, two USB2.0s shown in the rear panel, and two M.2 with 22*42 size storage connector. Rear I/O modules are available with following different I/O options:

Table 1.2: MIC-3332R1-S1E Configuration				
RTM Model Number	Rear Panel			
	LAN(RJ45)	VGA	USB 2.0	M.2 Storage (22*42 size)
MIC-332R1-S1E	2	1	2	2

1.2.13 Optional Extension Modules

MIC-3332 has two kinds of second layer. One 8HP XTM-1 is used for multi-display applications and also other rich I/O features; Another 8HP XTM-2 is used for multi-Ethernets applications. XTM connectivity is described in the list below. For a customized extension module demand, please contact Advantech local sales.

Table 1.3: The Second Layer 8HP XTM Configurations

8HP XTM	IO Panel				On-board Header/ Socket/Connector			
	LAN (RJ45/M12)	COM	HDMI	USB3.0	SATA	Cfast	Micro-SD	COM
8HP XTM-1 board	2	1	1	1	1	1	0	1
8HP XTM-2 board	4	0	0	0	1	1	1	0

1.2.14 Mechanical and Environmental Specifications

- **Operating temperature:** 0 ~ 55 °C (-32 ~ 131 °F)

> **Note!** *The operating temperature range of the MIC-3332 depends on the installed processor and the airflow through the chassis.*

- **Storage Temperature:** -40 ~ 85 °C (-40 ~ 185 °F)
- **Humidity:** 95% @ 40 °C (non-condensing)
- **Humidity (Non-operating):** 95% @ 60 °C (non-condensing)
- **Vibration:** 5~100Hz, 2Grms (without on-board 2.5" SATA HDD)
- **Shock:** 10G (without on-board 2.5" SATA HDD)
- **Board size:** 100 x 160 x 40.64 mm (3U size)
- **Weight:**
  3U 8HP FIO Board: 0.84 kg
  3U 4HP REAR IO Board (MIC-3332R1-S1E): 0.15kg

1.2.15 Compact Mechanical Design

Forced-air cooling in the chassis is recommended for MIC-3332 board to optimize its system stability and reliability even though there is a special Cu-designed heatsink assembled in unit already.

1.2.16 Hardware Monitor

For HWM management system in MIC-3332 series, In order to monitor processor temperature and core voltage information.

NCT7802Y is connected to SMBUS interface.

NCT7902D is optional function on MIC-3332 SKUs with 8HP XTM-1 board based on customer request, and used for FAN speed monitor and alarms.

NCT5523D also has optional functions on MIC-3332 SKUs with 8HP XTM-1 board based on customer request.

1.2.17 Super I/O

MIC-3332 Super I/O device can enable or disable serial ports, and you can select the serial port mode RS232/RS422/RS485 by jumper setting. For the details, please check item 1.4.

1.2.18 RTC and Battery

The RTC module keeps the date and time. On the MIC-3332 model the RTC circuitry is connected to battery sources.

1.3 Functional Block Diagram
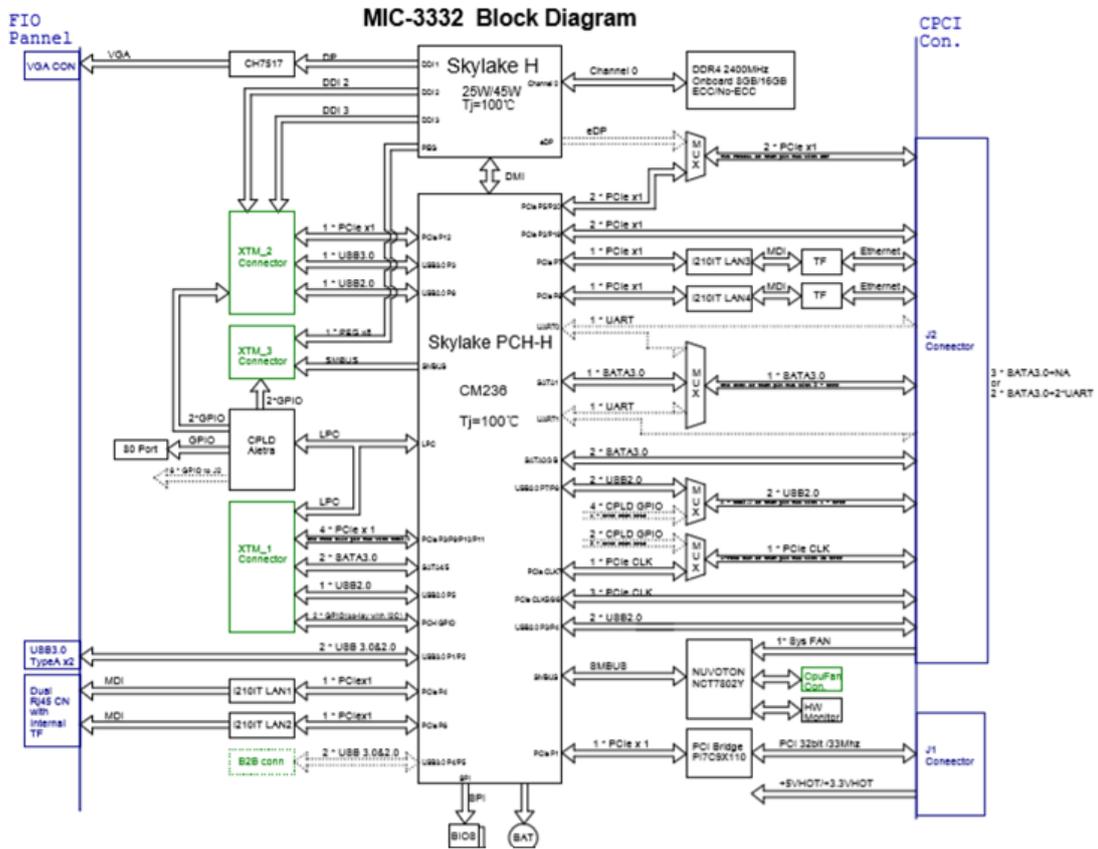
Figure 1.1 MIC-3332 functional block diagrams

1.4 Jumpers and Switches

For 1xRJ45 COM on 8HP XTM-1 Board, the default COM setting is RS-232. You can select COM mode by setting jumper as below table.

For 1x COM2 pin header on 8HP XTM-1 board, the default COM setting is also RS-232, and you can select COM mode by setting jumper as below table.
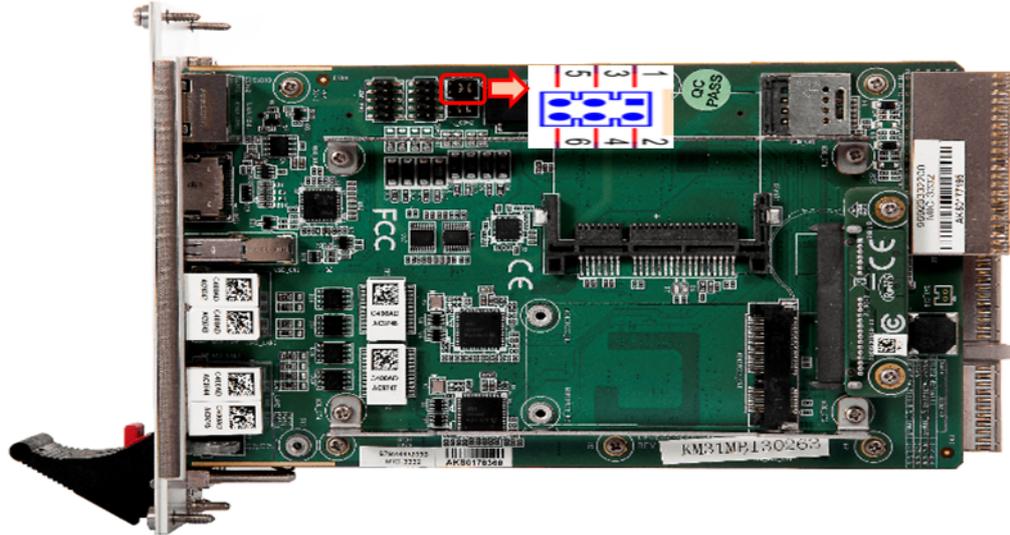
MO	M1	M2	JUMP-SEL	MODE
0	0	1	1-2, 3-4	Pure RS-232
1	0	0	CN(3-4), CN(5-6)	RS-422 With Term-R and Bias-R.
0	1	0	CN(1-2), CN(5-6)	RS-485
1	1	0	CN(1-3), CN(5-6)	RS-485 With Term-R and Bias-R.
1	1	1		Low Power Shutdown

Figure 1.2 MIC-3332 COM mode setting

1.5 Connector Definitions

Table 1.4 lists the function of each connector and Figure 1.3 and 1.4 illustrates each connector location.

Table 1.4: MIC-3332 on board connector descriptions (Front IO Board)		
Number	**Function**	**Note**
SATA1	SATA HDD daughter board	
CFast1	CFast Socket	
SD1	Micro-SD Connector (on MIC-3332 with 8HP XTM-2 board)	
J1	Primary CompactPCI Bus	
J2	Rear I/O Transition	

Table 1.5: MIC-3332 on board connector descriptions (Rear IO Board)		
Number	**Function**	**Note**
M2_CN1	M.2 connector	
M2_CN2	M.2 connector	

MIC-3332 series with 8HP(XTM-1) IO functions
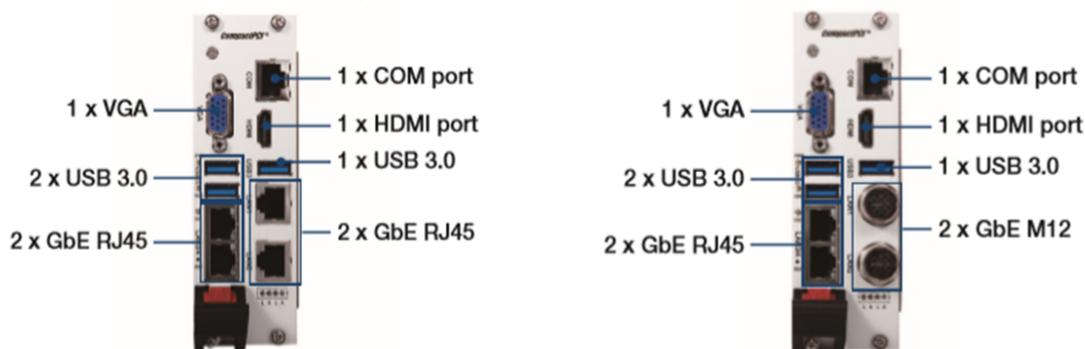
MIC-3332 series with 8HP(XTM-2) IO functions
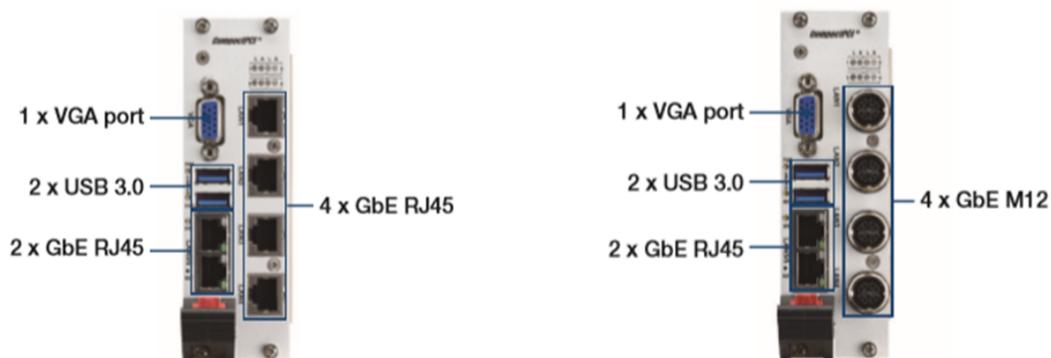
Figure 1.3 MIC-3332 Front Panel Ports, Indicators and Buttons

Figure 1.4 MIC-3332R1-S1E REAR IO Panel Ports and Indicators

1.6 Safety Precautions

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electric shock, always disconnect the power from your CompactPCI chassis before you work on it. Don't touch any components on the CPU board or other boards while the CompactPCI chassis is powered.
- Disconnect power before making any configuration changes. The sudden rush of power as you connect a jumper or install a board may damage sensitive electronic components.
- Always ground yourself to remove any static charge before you touch your CPU board. Be particularly careful not to touch the chip connectors.
- Modern integrated electronic devices, especially CPUs and memory chips, are extremely sensitive to static electric discharges and fields. Keep the board in its anti-static packaging when it is not installed in the chassis, and place it on a static dissipative mat when you are working with it. Wear a grounding wrist strap for continuous protection.

1.7 Installation Steps

The MIC-3332 contains electro-statically sensitive devices. Please discharge your clothing before touching the assembly. Do not touch components or connector pins. We recommend that you perform assembly at an anti-static workbench.

1.7.1 HDD/SSD Installation Steps

The MIC-3332 supports 2.5" SATA hard disk drive. The SATA HDD daughter board is assembled on the MIC-3332, but the SATA HDD brackets are not assembled on the MIC-3332. The brackets and screws are packed as accessories in the package. Following steps illustrate the installation of the SATA HDD.
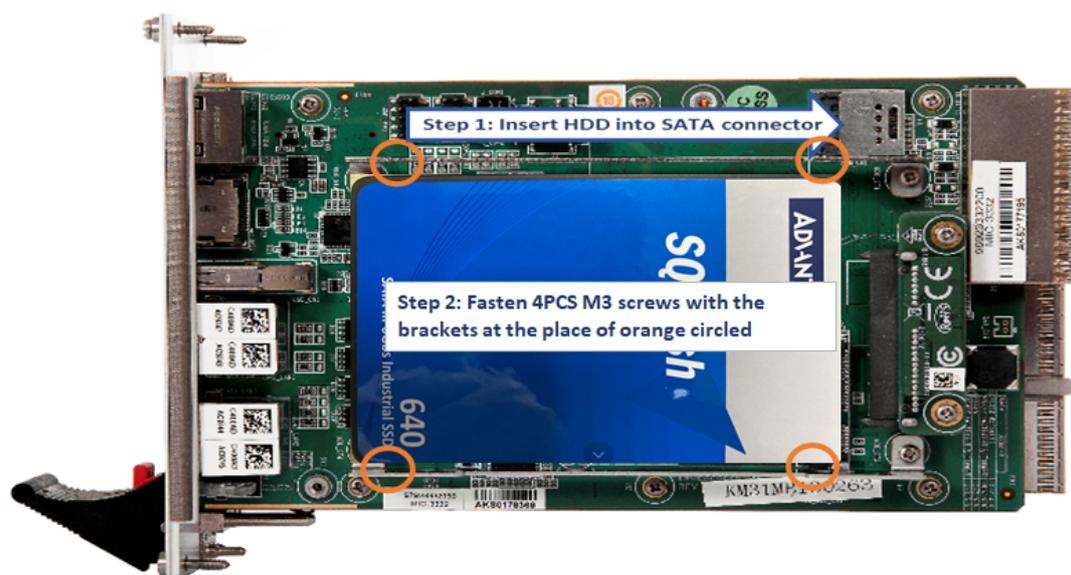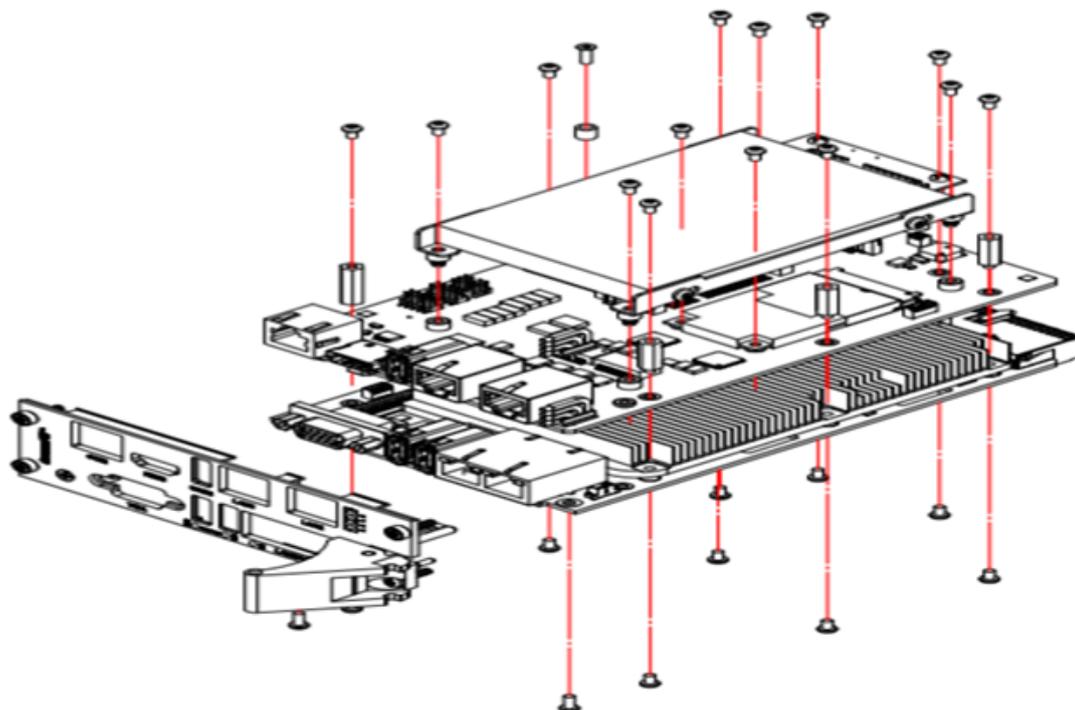
Figure 1.5 Assembly of MIC-3332 with 1 x 2.5" HDD/SSD

1.8 Battery Replacement

The battery model number is CR2032, 3V, 210 mAh battery with wire. Replacement batteries may be purchased from Advantech. When ordering the battery, please contact your local sales office to check availability.

1.9 Software Support

Windows 7, Windows 10, Ubuntu, CentOS 7.5, VxWorks 6.9/7.0 have been fully tested on the MIC-3332. Please contact representative for details on support for other operating systems.

Chapter 2

AMI BIOS Setup

This chapter describes how to configure the AMI BIOS.

2.1 Introduction

The AMI BIOS has been customized and integrated into many industrial and embedded motherboards for decades. This section describes the BIOS which has been specifically adapted for the MIC-3332. With the AMI UEFI BIOS Setup Utility, you can modify BIOS settings and control the special features of the MIC-3332. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter describes the basic navigation of the MIC-3332 setup screens.

```
                Aptio Setup Utility - Copyright (C) 2020 American Megatrends, Inc.
     Main Platform  Hardware  Post & Boot  Security  Save & Exit

    BIOS Information                                              Choose the system default
    BIOS Vendor                    American Megatrends            language
    Core Version                   5.11   0.41 x64
    Compliancy                     UEFI 2.4.0; PI 1.3
    Project Version                MIC-3332 V0.40
    Build Date and Time            08/05/2020 17:03:50
    NVRAM Version                  04.00
    CPLD Version                   FD.38


    System Language                [English]
    System Date                    [Wed 08/05/2020]
    System Time                    [09:29:24]
    Access Level                   Administrator                  ++: Select Screen
                                                                  ↑↓: Select Item
                                                                  Enter: Select
                                                                  +/-: Change Opt.
                                                                  F1: General Help
                                                                  F2: Previous Values
                                                                  F3: Optimized Defaults
                                                                  F4: Save & Exit
                                                                  ESC: Exit


                Version 2.18.1263. Copyright (C) 2020 American Megatrends, Inc.
```

Figure 2.1 Setup program initial screen

2.2 BIOS Setup

The MIC-3332 Series system has AMI BIOS built in, with a BIOS SETUP utility that allows users to configure required settings or to activate certain system features.

The BIOS SETUP saves the configuration in the NVRAM of the motherboard. When the power is turned off, the battery on the board supplies the necessary power. when CMOS battery is removed or the clear jumper is set, all user's settings will be restored the BIOS default settings.

When the power is turned on, press the <Del> or <F2> button during the BIOS POST (Power- On Self Test) to access the CMOS SETUP screen.

Control Keys

< → > < ← >	Select Screen
< ↑ > < ↓ >	Select item
<Enter>	Select
<+/->	Change Option
<F1>	General help, for Setup Sub Menu
<F2>	Previous values
<F3>	Optimized defaults
<F4>	Save & exit
<Esc>	Exit

2.3 Entering Setup

Turn on the computer, and there should be a POST (Power-On Self Test) screen that shows the CPU information. When pressing <DEL> or <F2>, you will immediately be allowed to enter Setup.

Figure 2.2 Setup Screen

2.3.1 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. Two main setup options are described in this section. The main BIOS setup screen is shown below.

```
                Aptio Setup Utility - Copyright (C) 2020 American Megatrends, Inc.
 Main  Platform  Hardware  Post & Boot  Security  Save & Exit

  BIOS Information                                         Choose the system default
  BIOS Vendor                American Megatrends           language
  Core Version               5.11   0.41 x64
  Compliancy                 UEFI 2.4.0; PI 1.3
  Project Version            MIC-3332 V0.40
  Build Date and Time        08/05/2020 17:03:50
  NVRAM Version              04.00
  CPLD Version               FD.38


  System Language            [English]
  System Date                [Wed 08/05/2020]
  System Time                [09:29:24]
  Access Level               Administrator             ►←: Select Screen
                                                       ↑↓: Select Item
                                                       Enter: Select
                                                       +/-: Change Opt.
                                                       F1: General Help
                                                       F2: Previous Values
                                                       F3: Optimized Defaults
                                                       F4: Save & Exit
                                                       ESC: Exit



                Version 2.18.1263. Copyright (C) 2020 American Megatrends, Inc.
```
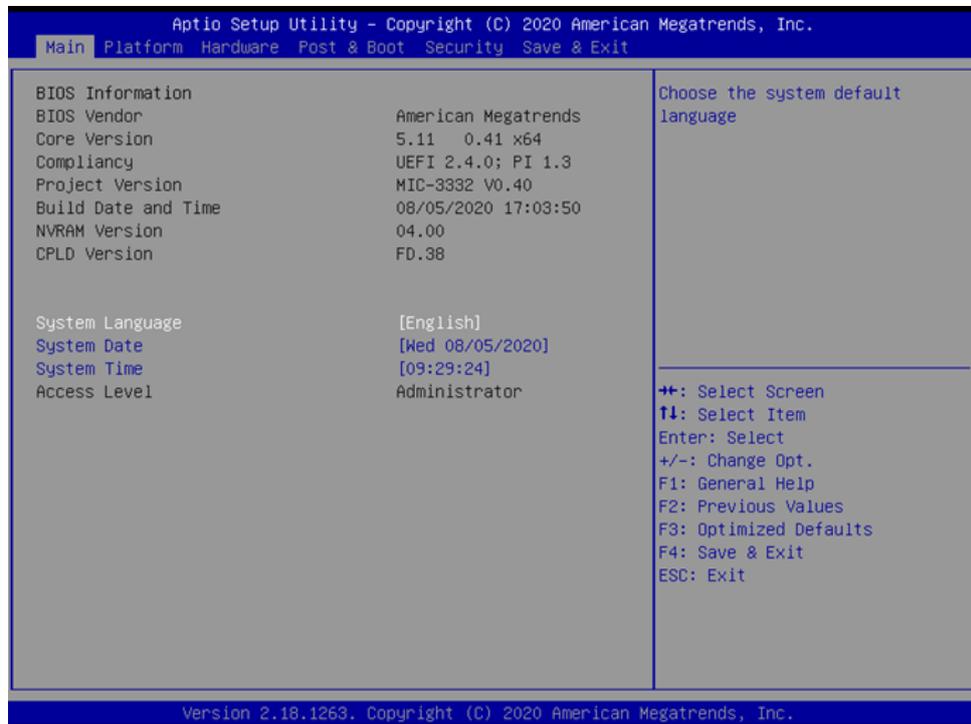
Figure 2.3 Main setup screen

The main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. The right frame displays the keyboard shortcuts. Above the keyboard shortcuts, there is an area reserved for a text message. When one option in the left frame is selected, it is highlighted in white. At the same time, the text message in the right frame always shows the further annotation.

■ **System Time/System Date**
Use this option to change the system time and date. Highlight System Time or System Date using the <↑><↓> keys. Input new values through the keyboard. Press the <↑><↓> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

2.3.2 Platform BIOS Features Setup

Select the Advanced tab from the MIC-3332 setup screen to enter the Advanced BIOS Setup screen. You can click one of the items in the left frame of the screen, such as serial console, to go to the sub menu of the selected item. You can display an platform option by highlighting it using the <↑><↓> keys. All the platform BIOS Setup options are described in this section. The platform BIOS Setup screen is shown below. The sub menus are described on the following pages.
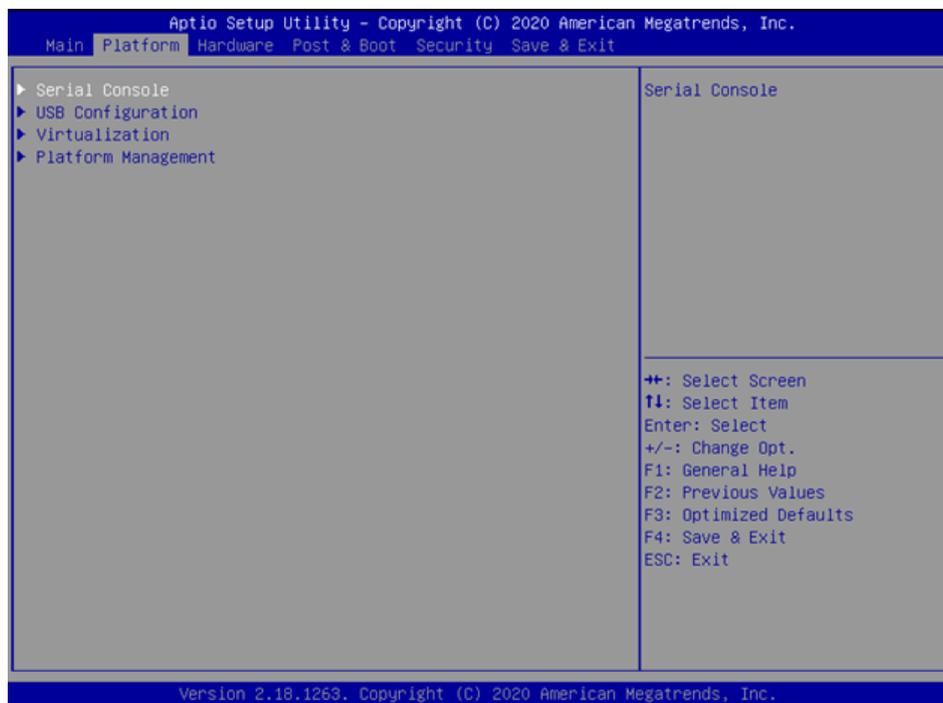

Figure 2.4 Platform BIOS features setup screen
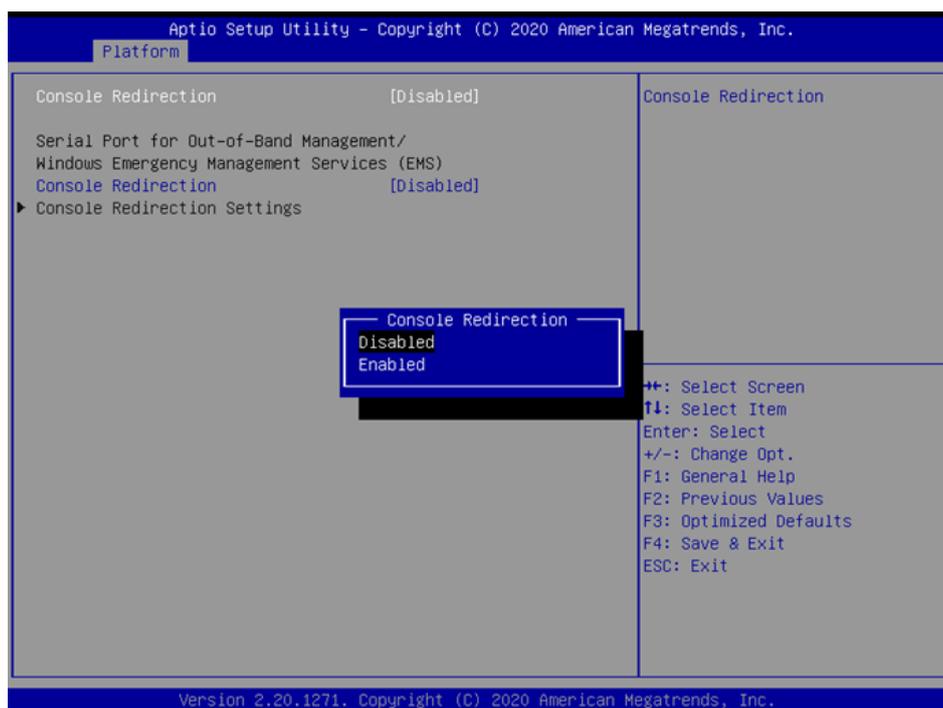
2.3.2.1 Serial Console Setting

Figure 2.5 Serial Console Setting

Serial console setting

- **Console Redirection**
  This item allows users to enable or disable console redirection or Microsoft Windows Emergency Management Services (EMS).

2.3.2.2 USB Configuration
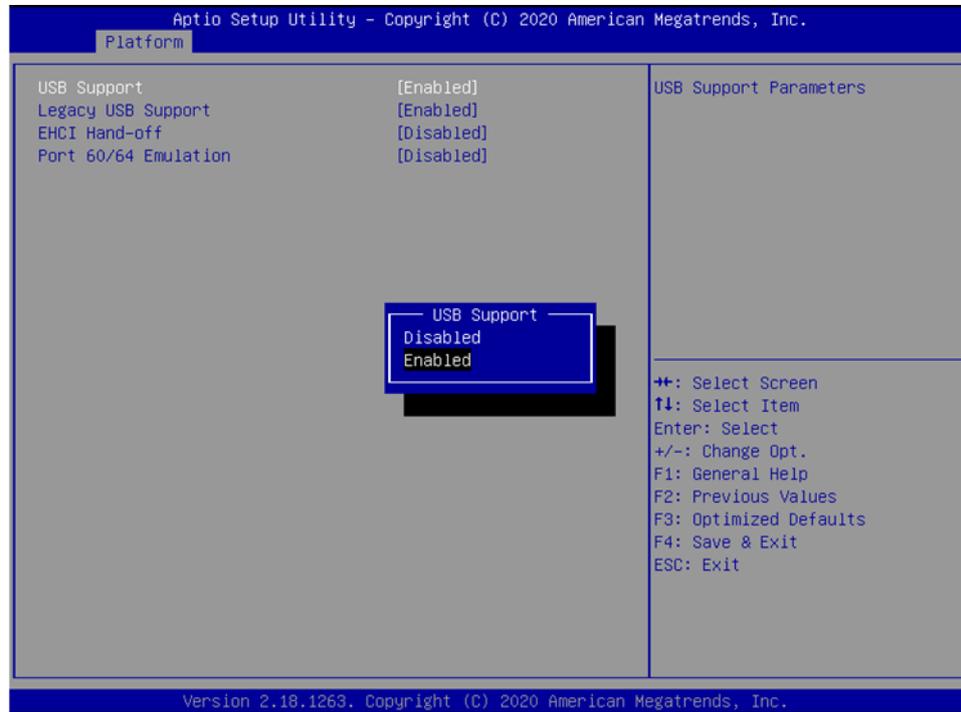
Figure 2.6 USB configuration

USB configuration setting

- **USB Support**
  USB support Parameters
- **Legacy USB support**
  Enables Legacy USB Support, AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.
- **EHCI Hand-off**
  This is a workaround for OS without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver
- **Port 60/64 Emulation**
  Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OS.

2.3.2.3 Virtualization
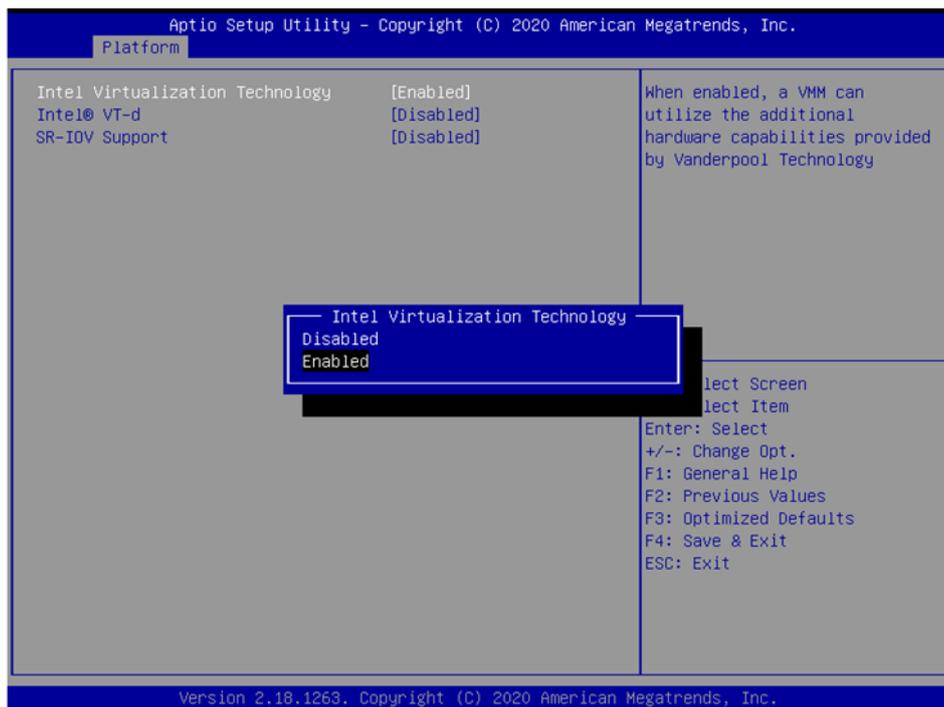
Figure 2.7 Virtualization

Virtualization Settings

■ **Intel (VMX) Virtualization Technology**
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology

■ **Intel®VT-d**
VT-d capability

■ **SR-IOV Support**
If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.

2.3.2.4 Platform Management
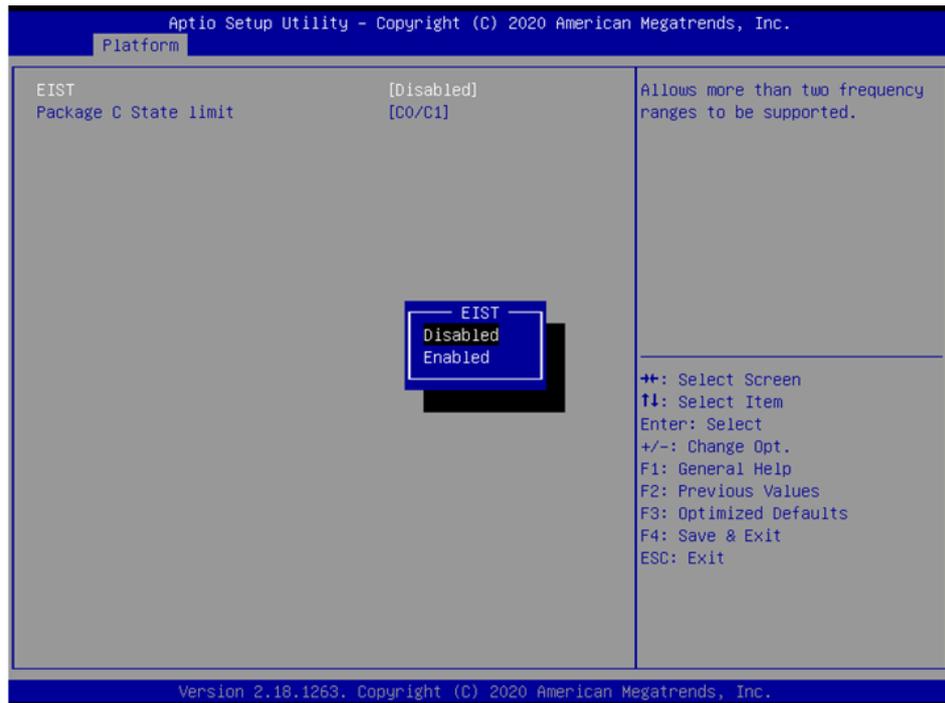
Figure 2.8 Platform Management

Platform management settings

- **EIST**
  Allows more than two frequency ranges to be supported.
- **Package C State Limit**
  Maximum Package C State Limit Setting.
  CPU Default: Leaves to Factory default value.
  Auto: Initializes to deepest available package C state Limit.

2.3.3 Hardware settings

Select the hardware tab from the BIOS setup screen to enter the Hardware Setup screen. Users can select any item in the left frame of the screen to go to the sub menu for that item. Users can display a Chipset Setup option by highlighting it using the <Arrow> keys. All hardware Setup options are described in this section. The hardware Setup screens are shown below. The sub menus are described on the following pages.
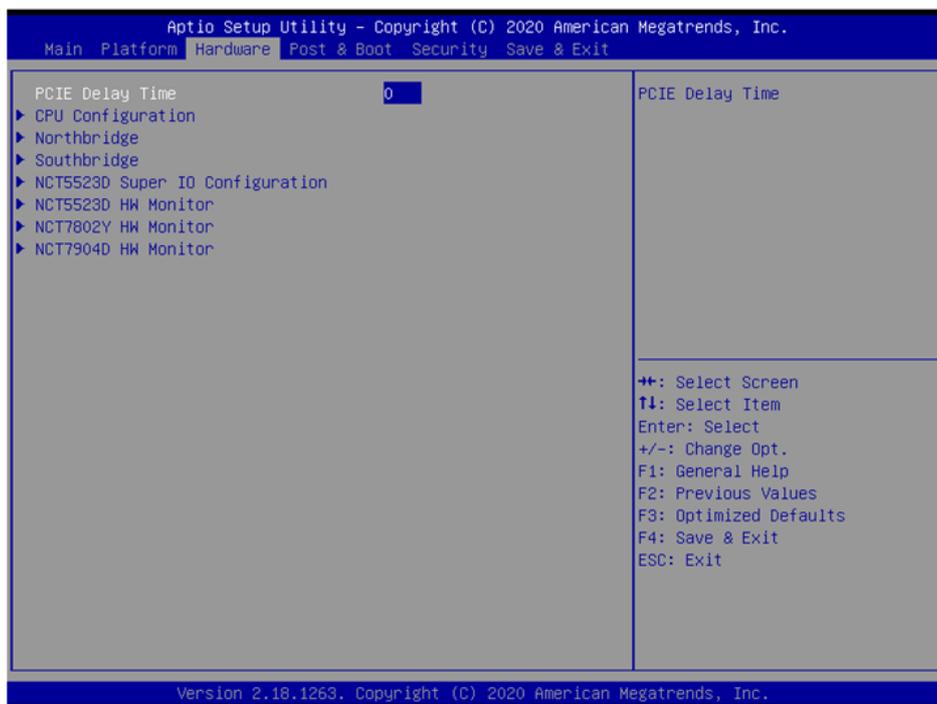
Figure 2.9 Hardware BIOS Setup Screen

2.3.3.1 CPU Configuration
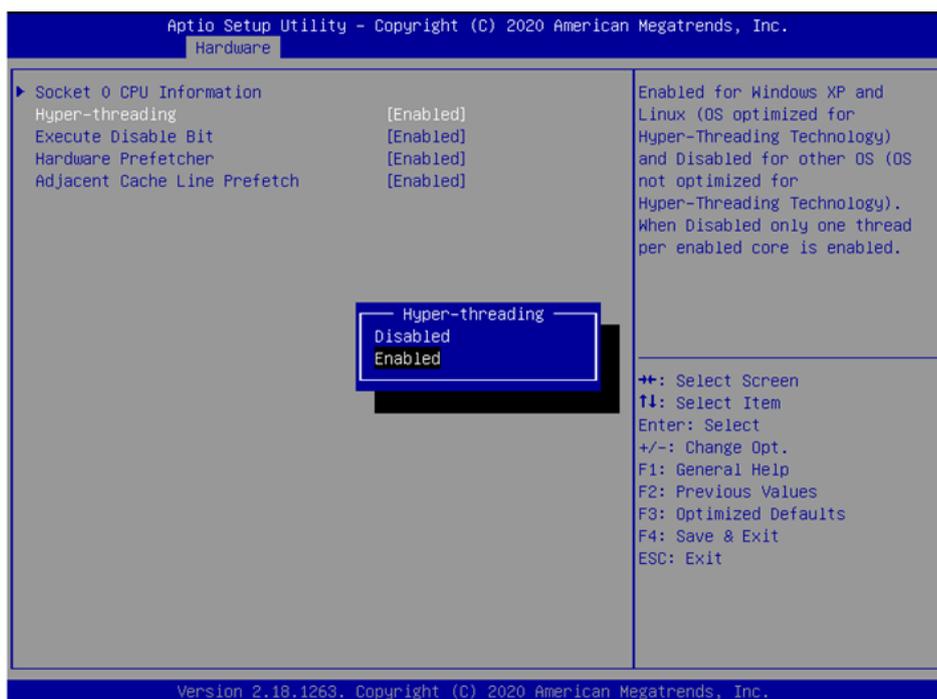
Figure 2.10 CPU Configuration

CPU configuration Settings

- **Hyper-Threading**
  Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology)
- **Execute Disable Bit**
  XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)
- **Hardware Prefetcher**
  To turn on/off the MLC streamer prefetcher
- **Adjacent Cache Line Prefetch**
  To turn on/off prefetching of adjacent cache lines

2.3.3.2 Northbridge

Figure 2.11 Northbridge

DIMM Information
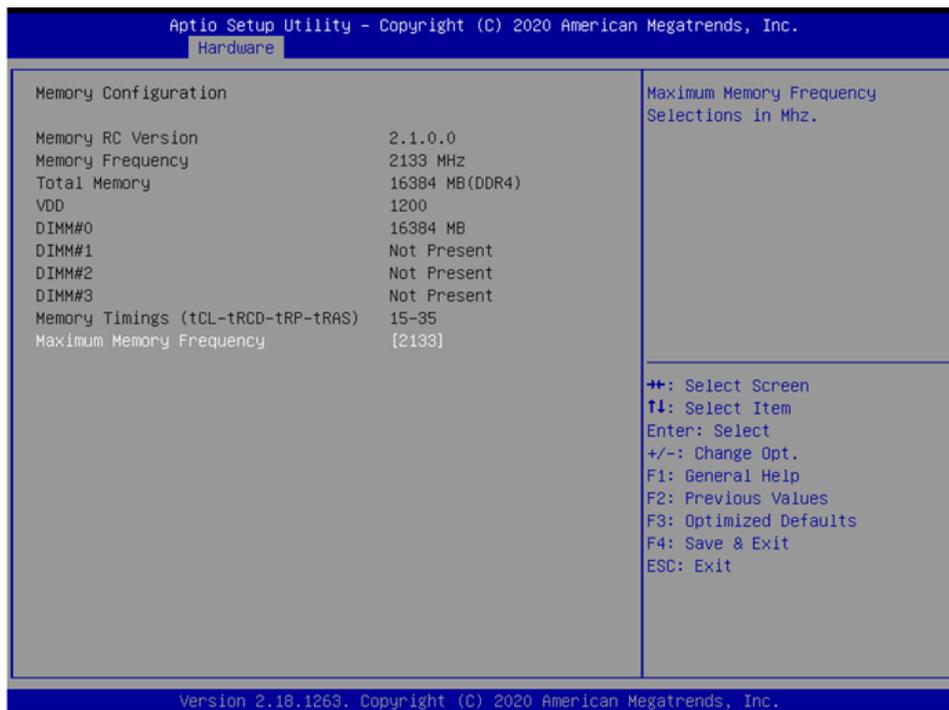
Figure 2.12 Memory Configuration

The option shows the memory information.

■ **PCI Subsystem Settings**
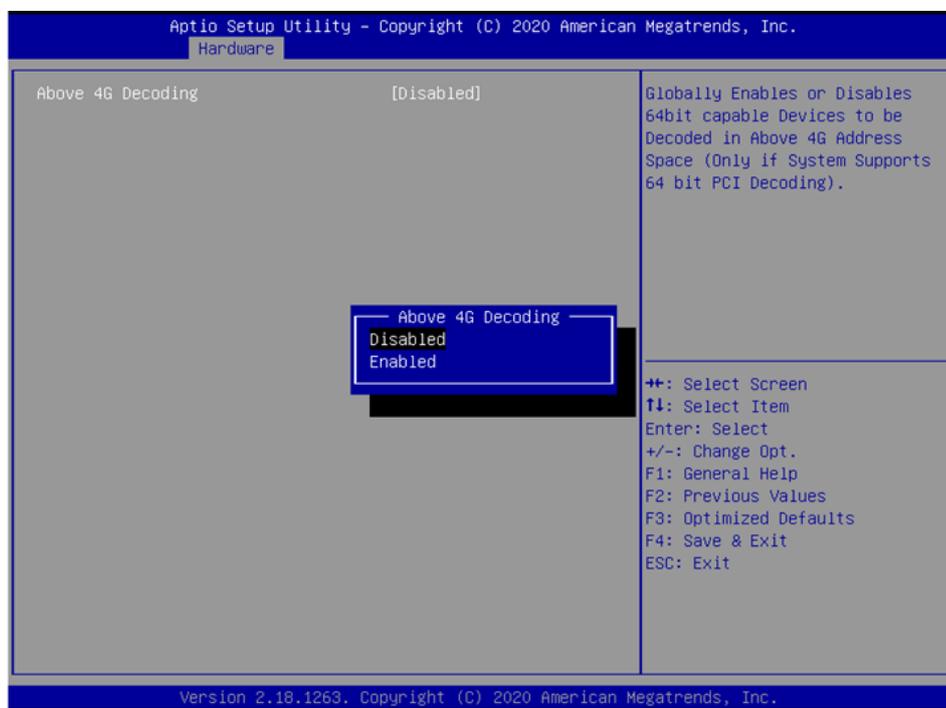
Figure 2.13 PCI Subsystem

– **Above 4G Decoding**
Enables or Disables 64-bit capable devices to be decoded in above 4G address space (only if system supports 64 bit PCI decoding).

2.3.3.3 Southbridge
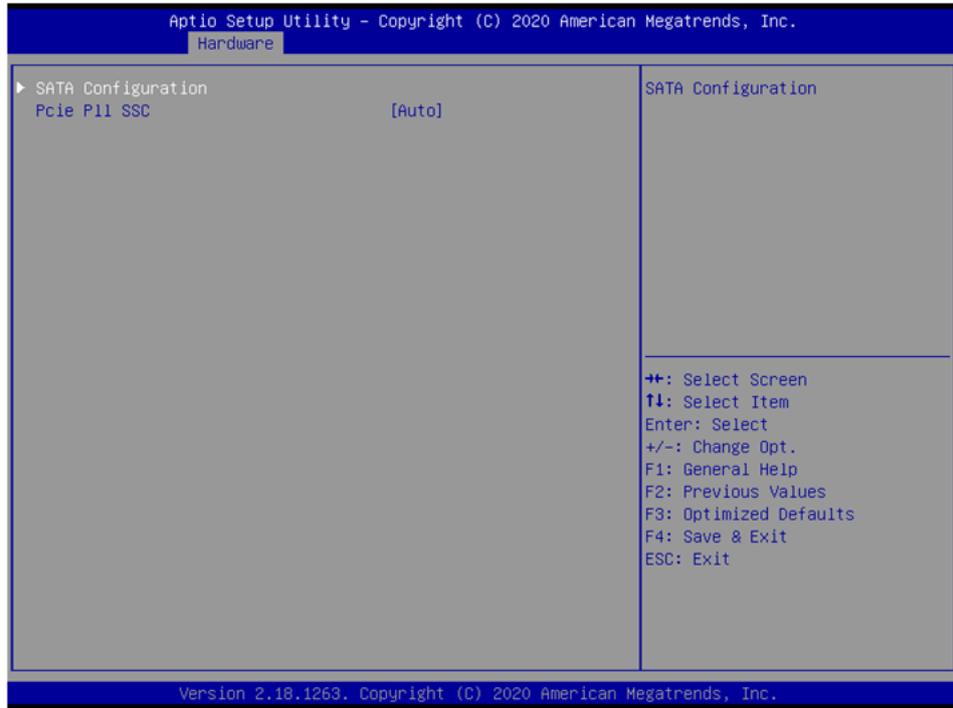
Figure 2.14 Southbridge

SATA Configuration
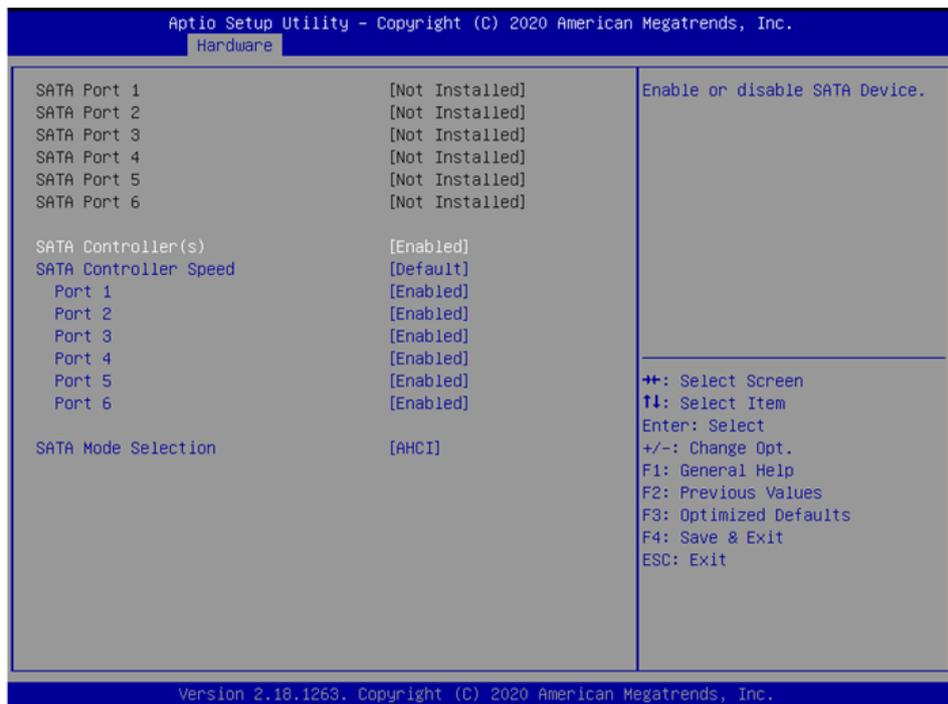
Figure 2.15 SATA Configuration

- **SATA Controller(s)**
  Enable/Disable SATA device
- **SATA Controller Speed**
  Indicates the maximum speed the SATA controller can support.
  Enable or Disable SATA port1/port2/port3/port4/port5/port6
- **SATA Mode Selection**
  Determines how SATA controller(s) operate.

2.3.3.4 NCT5523D Super IO Configuration
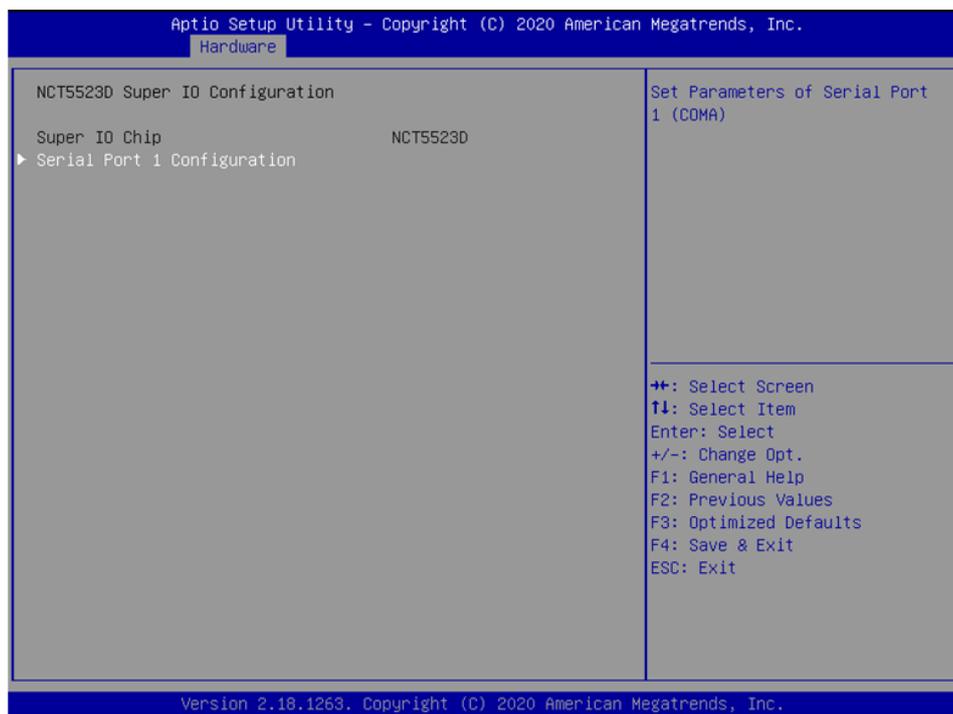
Figure 2.16 NCT5523D Super IO Configuration

Serial Port 1 configuration on 8HP XTM-1 board
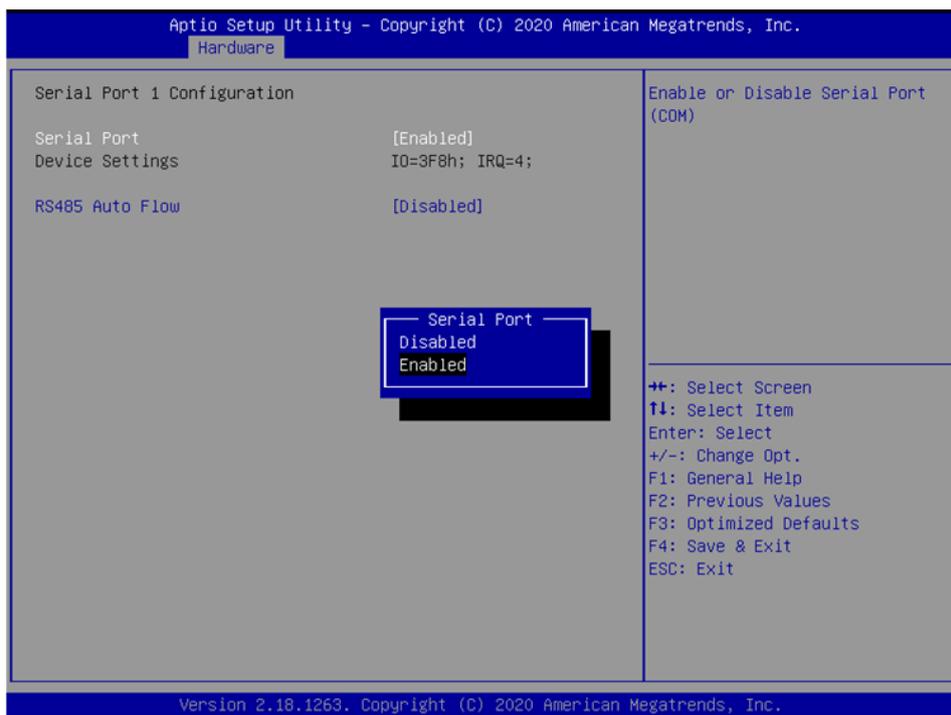
Figure 2.17 Serial Port1 Configuration

■ **Serial Port**
  – Enable or Disable Serial Port (COM);
  – When serial port mode is RS485, you can Enable or Disable "RS485 Auto Flow here.

2.3.3.5 NCT5523D H/W Monitor Configuration

Figure 2.18 NCT5523D H/W Monitor configuration

This option shows the Fan heath status.

2.3.3.6 NCT7802Y H/W Monitor Configuration
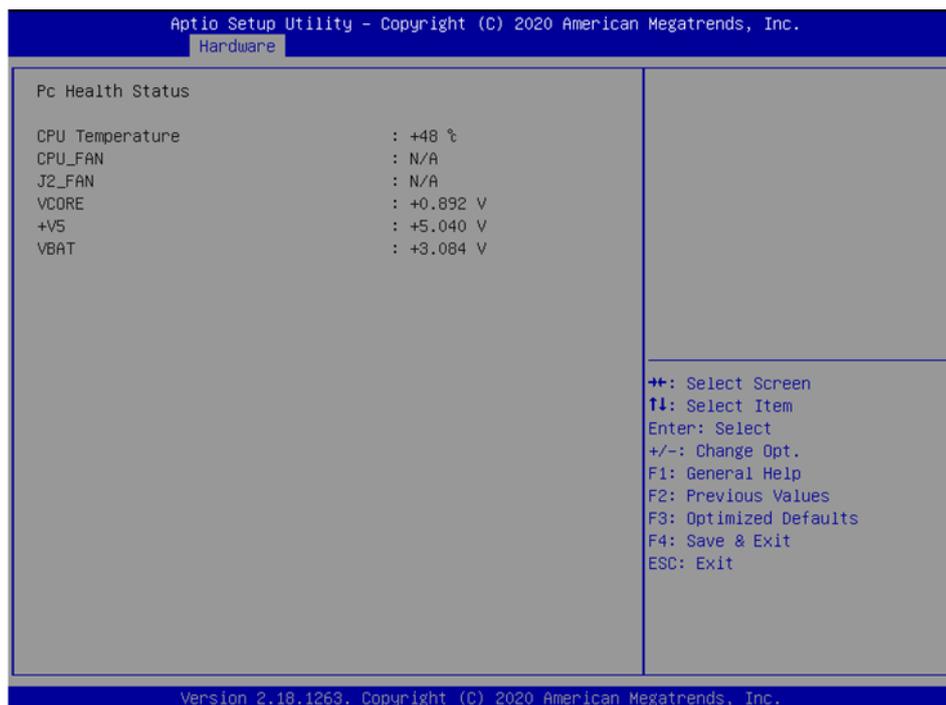
Figure 2.19 H/W Monitor configuration

This option shows PC heath status.

2.3.3.7 NCT7904 H/W Monitor Configuration

Figure 2.20 H/W Monitor configuration

This option shows the Fan health status. It only appears on MIC-3332 SKUs which with an XTM-1 board.

2.3.4 Post & Boot

Select the Post & Boot tab from the BIOS setup screen to enter the Post & Boot setup screen. Users can select any item in the left frame of the screen to go to the sub menu for that item. Users can display a Post & Boot Setup option by highlighting it using the <Arrow> keys. All Post & Boot Setup options are described in this section. The Setup screens are shown below. The sub menus are described on the following pages.

```
            Aptio Setup Utility - Copyright (C) 2020 American Megatrends, Inc.
      Main  Platform  Hardware  Post & Boot  Security  Save & Exit

    Setup Prompt Timeout              1                    Number of seconds to wait for
    Bootup NumLock State              [On]                 setup activation key.
    Quiet Boot                        [Disabled]           65535(0xFFFF) means indefinite
    Network Stack                     [Disabled]           waiting.

    Boot Option Priorities
    Boot Option #1                    [UEFI: Built-in EFI
                                      Shell]
    Boot Option #2                    [KingstonDataTraveler
                                      3.0PMAP]
    Boot Option #3                    [UEFI:
                                      KingstonDataTraveler
                                      3.0PMAP, Partition 1]

    Hard Drive BBS Priorities                              →←: Select Screen
                                                           ↑↓: Select Item
  ▶ CSM16 Parameters                                       Enter: Select
  ▶ CSM Parameters                                         +/-: Change Opt.
                                                           F1: General Help
                                                           F2: Previous Values
                                                           F3: Optimized Defaults
                                                           F4: Save & Exit
                                                           ESC: Exit

              Version 2.18.1263. Copyright (C) 2020 American Megatrends, Inc.
```
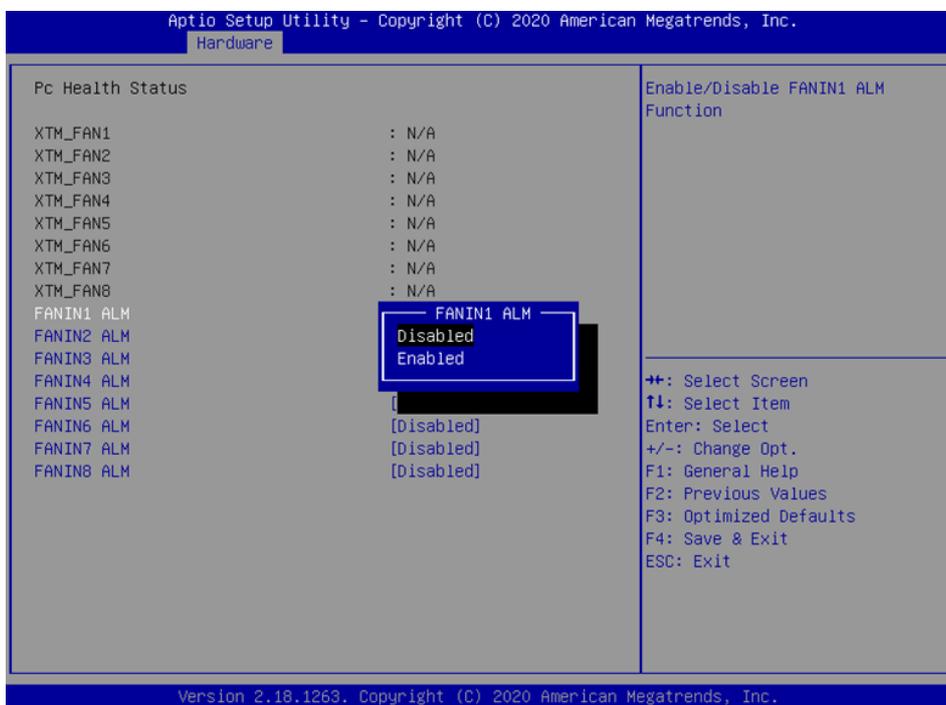
Figure 2.21 Post & Boot Setup Screen

Post & Boot Settings

- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key.
  65535 (oxFFFF) means indefinite waiting.
- **Boot up NumLock State**
  Select the keyboard NumLock state. By "ON", the keyboard NumLock state will stay "ON" after booting. By "OFF", the keyboard NumLock state will stay "OFF" after booting.
- **Quiet Boot**
  Enable or disable quiet boot option. If this option is set to Disabled, the BIOS displays normal POST messages. If enabled, an OEM Logo is shown instead of POST messages.
- **Network Stack**
  Enable/Disable UEFI Network Stack
- **Boot Option**
  Boot Option #1
  Boot Option #2
  Boot Option #3
  The option shows the boot priority of devices.
- **Hard Drive BBS Priorities**
  Set boot device priority sequence from available hard disk drives.

■ **CSM16 Parameters**
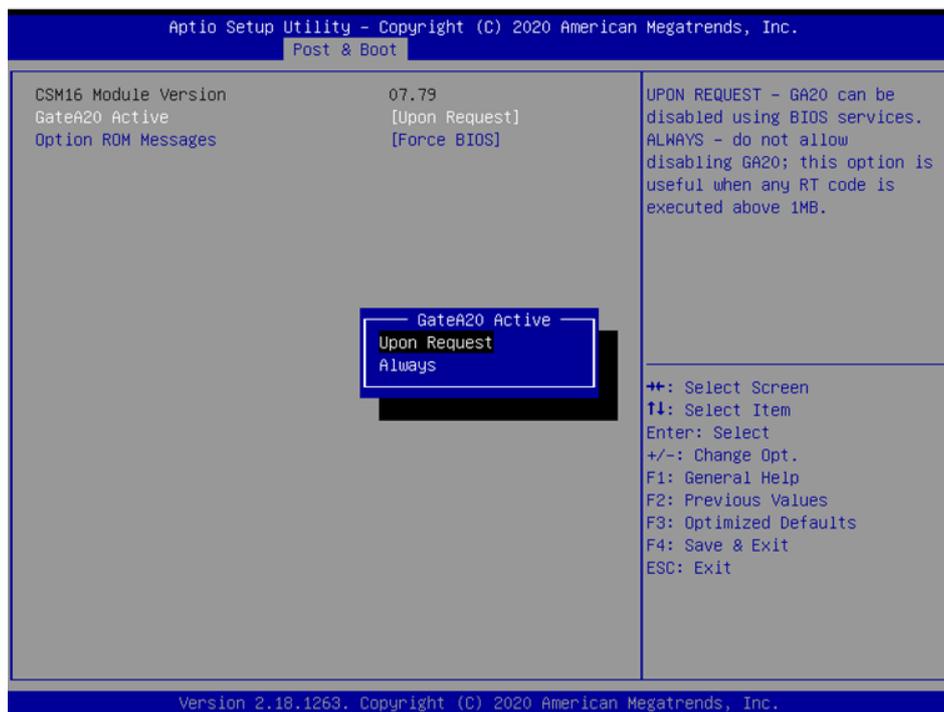
Figure 2.22 CSM16 Parameters

This item allows users to set display mode for Option ROM.

GateA20 Active:

UPON REQUEST: GA20 can be disabled using BIOS services.

ALWAYS: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

■ **CSM Parameters**
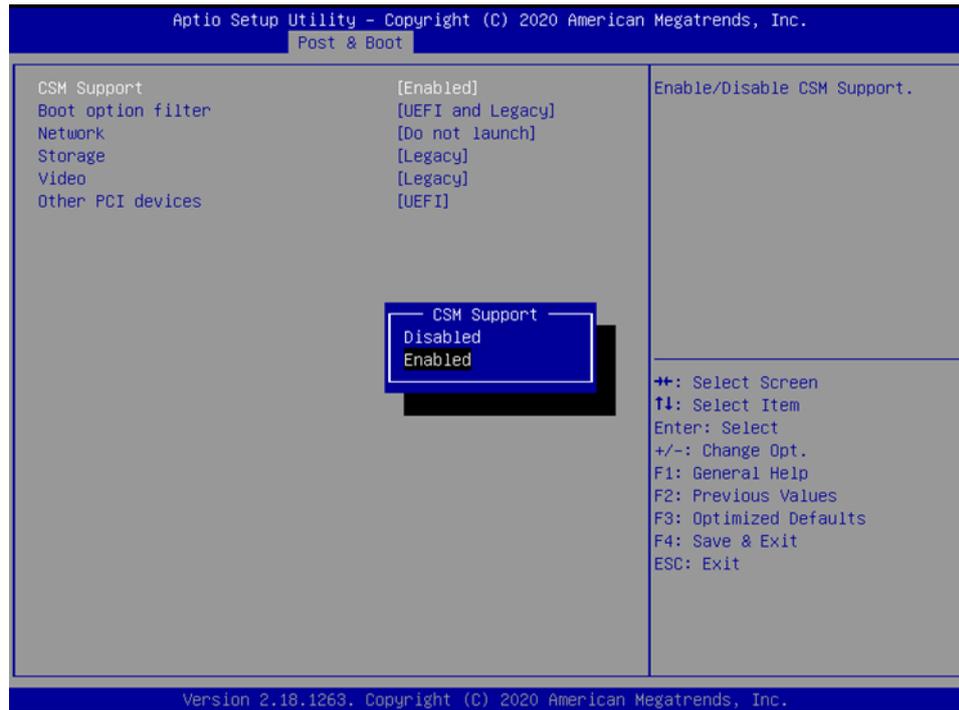
Figure 2.23 CSM Parameters

This option controls if CSM will be launched.

- ■ CSM Support: Enable/Disable CSM Support.
- ■ Boot option filter: This option controls Legacy/UEFI ROMs priority.
- ■ Network: Controls the execution of UEFI and Legacy PXE Option.
- ■ Storage: Controls the execution of UEFI and Legacy Storage OpROM.
- ■ Video: Controls the execution of UEFI and Legacy Video OpROM.
- ■ Other PCI devices: Determines OpROM execution policy for devices other than Network,Storage,or Video.

2.3.5 Security
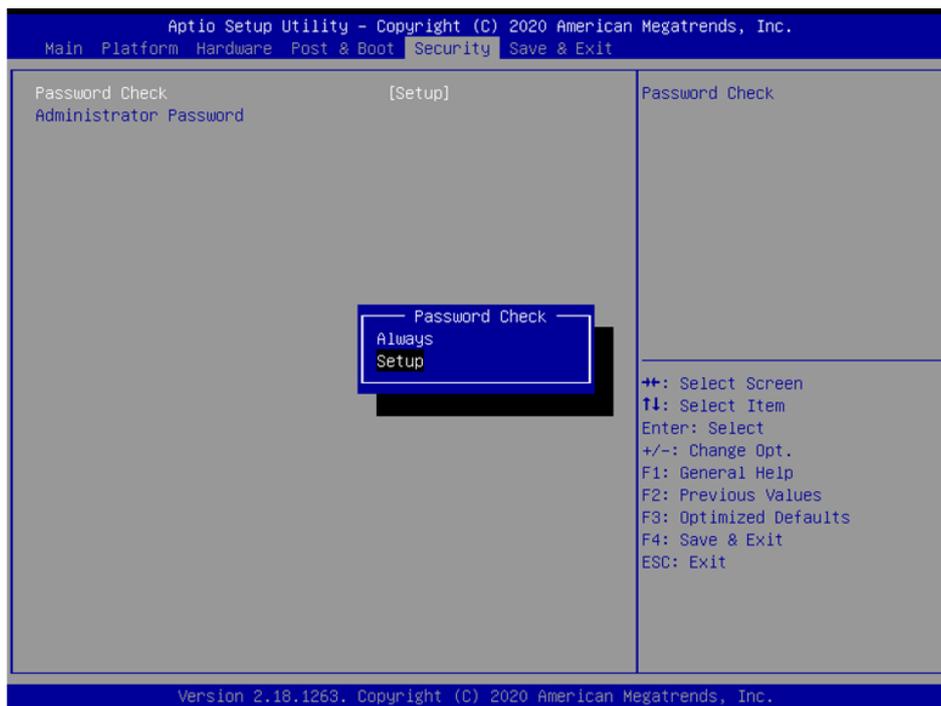
Figure 2.24 Security Settings

■ **Password Check**
   – Password Check: Set Password check mode.
   – Administrator Password: Set Administrator Password

2.3.6 Save & Exit
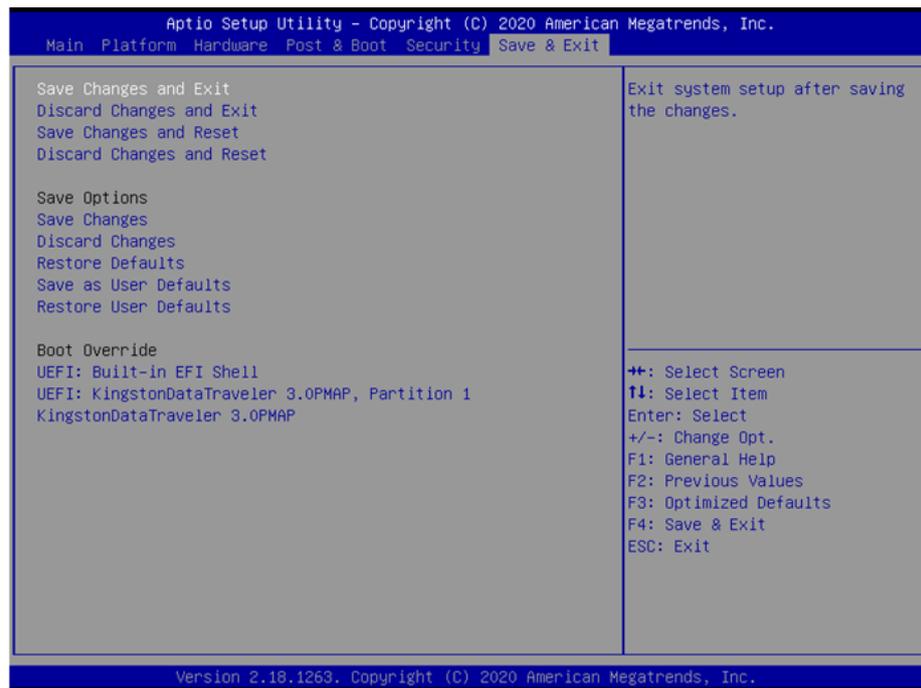
Figure 2.25 Save & Exit

■ **Save Changes and Exit**
When users have completed system configuration, select this option to save changes, exit BIOS setup menu and reboot the computer to take effect all system configuration parameters.
1. Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [OK] [Cancel]
2. Select OK or cancel.

■ **Discard Changes and Exit**
Select this option to quit Setup without making any permanent changes to the system configuration.
1. Select Exit Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [OK] [Cancel]
2. Select OK to discard changes and exit. Discard Changes: Select Discard Changes from the Exit menu and press <Enter>.

■ **Save Changes and Reset**
Reset the system after saving the changes.

■ **Discard Changes and Reset**
Reset system setup without saving any changes.

■ **Save changes**
Save changes done so far to any of the setup options.

■ **Discard Changes**
Discard Changes done so far to any of the setup options.

■ **Restore Default**
The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not

use the Defaults if the user's computer is experiencing system configuration problems. Select Restore Defaults from the Exit menu and press <Enter>.

■ **Save as User Default**
Save the all current settings as a user default.

■ **Restore User Default**
Restore all settings to user default values.

■ **Boot Override**
This option shows the boot device for you to choose.

Appendix A

Pin Assignments

This appendix describes pin assignments.

A.1 J1 Connector

Pin	A	B	C	D	E	F
Table A.1: J1 CompactPCI I/O						
1	+5V_HOT	NC	TRST#	NC	+5V_HOT	GND
2	TCK	+5V_HOT	TMS	TDO	TDI	GND
3	INTA#	INTB#	INTC#	+5V_HOT	INTD#	GND
4	NC	HEALTHY#_R	CPCI_VIO	INTP	INTS	GND
5	NC	NC	RST#_R	GND	GNT#0	GND
6	REQ#0	B6 (CPCI_VIO PU)	+3V_HOT	CLK0	AD31	GND
7	AD30	AD29	AD28	GND	AD27	GND
8	AD26	GND	CPCI_VIO	AD25	AD24	GND
9	CBE#3	IDSEL	AD23	GND	AD22	GND
10	AD21	GND	+3V_HOT	AD20	AD19	GND
11	AD18	AD17	AD16	GND	CBE#2	GND
12						NC
13			KEY Area			GND
14						NC
15	+3V_HOT	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
16	DEVSEL#	PCIXCAP	CPCI_VIO	STOP#	LOCK#	GND
17	+3V_HOT	SCL	SDA	GND	PERR#	GND
18	SERR#	GND	+3V_HOT	PAR	CBE#1	GND
19	+3V_HOT	AD15	AD14	GND	AD13	GND
20	AD12	GND	CPCI_VIO	AD11	AD10	GND
21	+3V_HOT	AD9	AD8	J1_M66EN	CBE#0	GND
22	AD7	GND	+3V_HOT	AD6	AD5	GND
23	+3V_HOT	AD4	AD3	+5V_HOT	AD2	GND
24	AD1	+5V_HOT	CPCI_VIO	AD0	ACK64#	GND
25	+5V_HOT	RQ64	ENUM#_R	+3V_HOT	+5V_HOT	GND

Note!   *NC: No Connection*

#: Active Low

A.2 J2 Connector

Pin	A		B		C		D		E		
Table A.2: J2 CompactPCI I/O											
SKU	Plus IO	Non Plus IO	Plus IO	Non Plus IO	Plus IO	Non Plus IO	Plus IO	Non Plus IO	Plus IO	Non Plus IO	F
1	CLK1	CLK1	GND	GND	REQ#1	REQ#1	GNT#1	GNT#1	REQ#2	REQ#2	GND
2	CLK2	CLK2	CLK3	CLK3	SYSEN#	SYSEN#	GNT#2	GNT#2	REQ#3	REQ#3	GND
3	CLK4	CLK4	GND	GND	GNT#3	GNT#3	REQ#4	REQ#4	GNT#4	GNT#4	GND
4	CPCI_VIO	CPCI_VIO	PCIE_TXN1	PCIE_TXN1(GEN1)	USB2_N1	USB2_N1	NC	UART1_CTS#	+V5SB	+V5SB	GND
5	PCIE_RXN1	PCIE_RXN1(Gen1)	PCIE_TXP1	PCIE_TXP1(Gen1)	USB2_P1	USB2_P1	NC	UART1_RXD	NC	UART2_CTS#	GND
6	PCIE_RXP1	PCIE_RXP1(Gen1)	PCIE_TXN2	EDP_TX2-	USB2_N2	USB2_N2	SATA_TXN2	UART1_RTS#	NC	UART2_RXD	GND
7	PCIE_RXN2	EDP_TX0-	PCIE_TXP2	EDP_TX2+	USB2_P2	USB2_P2	SATA_TXP2	UART1_TXD	SATA_RXN2	UART2_RTS#	GND
8	PCIE_RXP2	EDP_TX0+	PCIE_TXN3	PCIE_TXN3(Gen1)	USB2_N3	GPIO4	SATA_TXN3	SATA_TXN3(Gen2)	SATA_RXP2	UART2_TXD	GND
9	PCIE_RXN3	PCIE_RXN3(Gen1)	PCIE_TXP3	PCIE_TXP3(Gen1)	USB2_P3	GPIO3	SATA_TXP3	SATA_TXP3(Gen2)	SATA_RXN3	SATA_RXN3(Gen2)	GND
10	PCIE_RXP3	PCIE_RXP3(Gen1)	PCIE_TXN4	EDP_TX3-	USB2_N4	GPIO2	SATA_TXN4	SATA_TXN4(Gen2)	SATA_RXP3	SATA_RXP3(Gen2)	GND
11	PCIE_RXN4	EDP_TX1-	PCIE_TXP4	EDP_TX3+	USB2_P4	GPIO1	SATA_TXP4	SATA_TXP4(Gen2)	SATA_RXN4	SATA_RXN4(Gen2)	GND
12	PCIE_RXP4	EDP_TX1+	PCIE1_CLKE#	PCIE1_CLKE#	PCIE2_-CLKE#	PCIE2_-CLKE#	eDP_HPC_$	eDP_HPD_R	SATA_RXP4	SATA_RXP4(Gen2)	GND
13	PCIE_CLK3+	PCIE_CLK3+	PCIE_CLK1-	PCIE_CLK1-	PCIE3_-CLKE#	PCIE3_-CLK#	LANA_LINK-ACT#	LANA_LINK-ACT#	LANB_LINK-ACT#	LANB_LINK-ACT#	GND
14	PCIE_CLK3-	PCIE_CLK3-	PCIE_-CLK1+	PCIE_CLK1+	PCIE4_-CLKE#	PCIE_-CLKE#	LANA_LINK1000#_100#	LANA_LINK1000#_100#	HWM_FANIN2	HWM_FANIN2	GND
15	PCIE_CLK4+	GPIO6	PCIE_CLK2-	eDP_AUX-	FAL#	FAL#	REQ#5	REQ#5	GNT#5	GNT#5	GND
16	PCIE_CLK4-	GPIO5	PCIE_CLK2+	eDP_AUX+	DEG#	DEG#	GND	GND	HWM_PWMOUT2/LANB_LINK_1000#_100#	HWM_PWMOUT2/LANB_LINK1000#_100#	GND
17	LANB MDI3-	LANB MDI3-	LANB MDI2-	LANB_MDI2-	PRST#	PRST#	REQ#6	REQ#6LANA_MDI2-	GNT#6	GNT#6	GND
18	LANB MDI3+	LANB MDI3+	LANB MDI2+	LANB_MDI2+	LANB_MDI0-	LANB_MDI0-	LANA_MDI2-	LANA_MDI2+	LANA_MDI0-	LANA_MDI0-	GND
19	GND	GND	GND	GND	LANB_MDI0+	LANB_MDI0+	LANA_MDI2+	LANA_MDI3-	LANA_MDI0+	LANA_MDI0+	GND
20	CLK5	CLK5	GND	GND	LANB_MDI1-	LANB_MDI1-	LANA_MDI3-	LANA_MDI3-	LANA_MDI1-	LANA_MDI1-	GND
21	CLK6	CLK6	GND	GND	LANB_MDI1+	LANB_MDI1+	LANA_MDI3+	LANA_MDI3+	LANA_MDI1+	LANA_MDI1+	GND
22	GA4	GA4	GA3	GA3	GA2	GA2	GA1	GA1	GA0	GA0	GND

Note! NC: No Connection

#: Active Lo

Table A.3: VGA1 Connector			
1	RED	9	+5V
2	GREEN	10	GND
3	BLUE	11	NC
4	NC	12	DDC_DATA
5	DET#	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDC_CLK
8	GND		

Table A.4: RJ45 LAN1/LAN2 Connector on 4HP board			
1	LAN_0+	5	LAN_2-
2	LAN_0-	6	LAN_1-
3	LAN_1+	7	LAN_3+
4	LAN_2+	8	LAN_3-
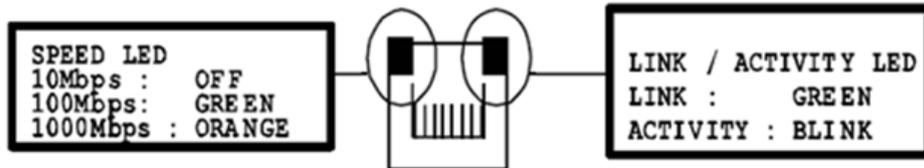
Table A.5: RJ45 LAN1/LAN2 Connector on 8HP XTM-1 Board & RJ45 LAN1~LAN4 Connector on 8HP XTM-2 Board			
1	LAN_MDI0+	5	LAN_MDI2-
2	LAN_ MDI0-	6	LAN_ MDI1-
3	LAN_ MDI1+	7	LAN_ MDI3+
4	LAN_ MDI2+	8	LAN_ MDI3-
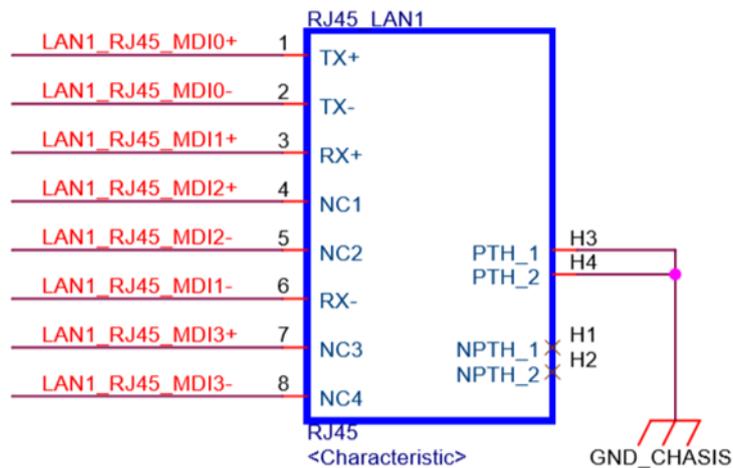
Table A.6: M12 LAN1/LAN2 Connector on 8HP XTM-1 Board & M12 LAN1~LAN4 Connector on 8HP XTM-2 Board

1	LAN_ MDI0+	5	LAN_ MDI3+
2	LAN_ MDI0-	6	LAN_ MDI3-
3	LAN_ MDI1+	7	LAN_ MDI2-
4	LAN_ MDI1-	8	LAN_ MDI2+
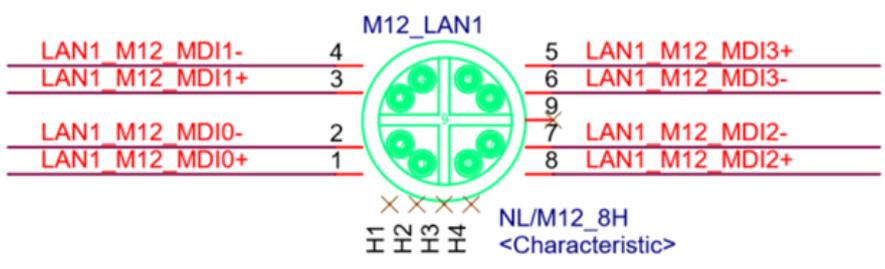
Table A.7: USB3CN1(4HP), USB3CN2(4HP), USB3_CN1(8HP XTM-1 Board)

USB3CN1&USB3CN2 on 4HP Board, USB3_CN1 on 8HP XTM-1 Board

1	+5V (fused)
2	USBD-
3	USBD+
4	GND
5	SSRX-
6	SSRX+
7	GND
8	SSTX-
9	SSTX+

Table A.8: COM1 (RJ45) Connector on 8HP XTM-1 Board

1	TX+	5	GND
2	TX-	6	DSR#
3	RX+	7	RTS#
4	RX-	8	CTS#

Table A.9: BAT_CN CMOS battery

1	BAT_VCC	2	GND

A.3 M/D, PWR, HDD, Hot-swap & LAN LEDs

Twelve LEDs are provided on the front panel as follows:

Table A.10: Front Panel LEDs Indication		
Layer	**Name**	**Description**
4HP	PWR (Green)	Indicates power status
	HDD (Yellow)	Indicates HDD Read/Write
	H/S (Blue)	Indicates the board is ready to be hot-swapped
	Master/Drone (Blue)	Blue blink Indicates the board is inserted into peripheral slots
8HP XTM	LAN (Link)	1000Mb/s :Orange , 100Mb/s: Green;10Mb/s: LED off
	LAN (Activity)	Green Blink

Appendix B

Programming the Watchdog Timer

This appendix describes how to program the watchdog timer.

Watchdog function can be used by customer through IO access changing registers of 0x443h and 0x444h.

Register Address: IO address 443h
Register Name: Watchdog Count Value
Default Value: 00
Attribute: Read/Write

Bit	Description	Access
7-0	Watchdog Count Value (default unit:sec)	RW

Register Address: IO address 444h
Register Name: Watchdog Function
Default Value: 80
Attribute: Read/Write

Bit	Description	Access
7	1: dual BIOS enable (default) 0: dual BIOS disable	RO
6:3	Reserved	RO
2:1	00: unit:sec(default) 01: unit:min 10: unit:hour 11: unit:day	RW
0	1: Watchdog Enable 0: Watchdog Disable (default)	RW

Note:

- Watchdog don't work, until bit 0 of 0x444h is set to 1.
- Customer can set Watchdog Count Value register firstly, then enable Watchdog and set Watchdog value counter unit.
- If Watchdog counter timing out , it will cause system reset by pull low system_reset pin of PCH for 20ms.

For example:

Filling 0x20(0010 0000) in 0x443h through IO access, then filling 0x03(0000 0011) in 0x444h through IO access.System will reboot after 32 minute.

- Bit 7 is default high: it will call watchdog function to ensure system can power on successfully.

Appendix C

FPGA Specification

This appendix describes FPGA configuration.

C.1 Overview

For the MIC-3332 project, a CPLD (10M02SCU169I7G) from the Altera Max 10 family is used.

C.1.1 CPLD Functional Blocks
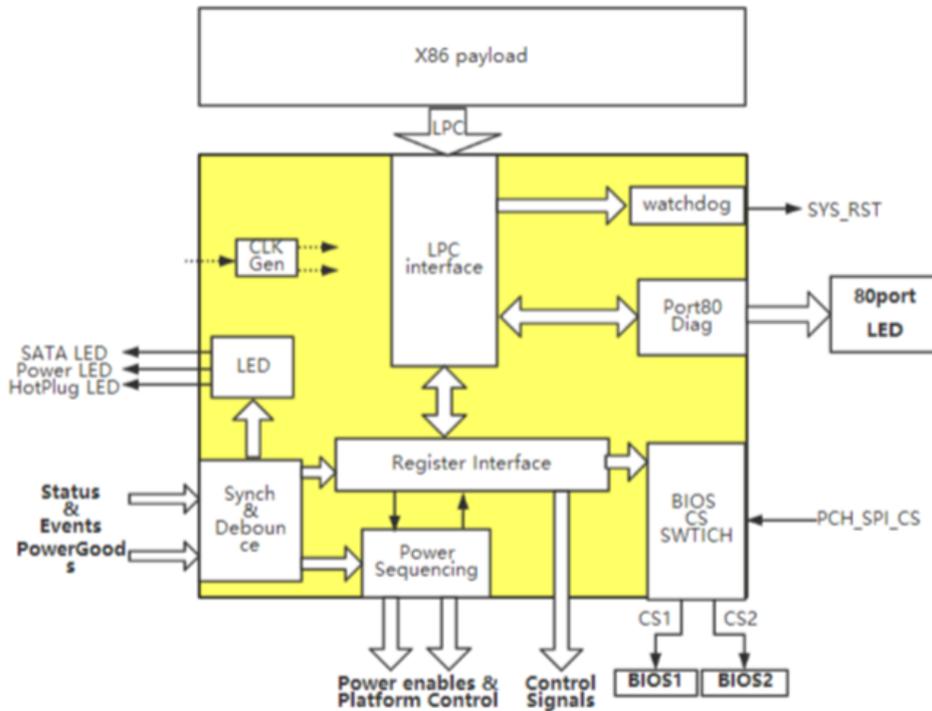
Figure C.1 CPLD Block Diagram

C.2 Features

The following functional blocks are realized inside the CPLD:

- LPC interface
  - Connects the LPC bus to the CPLD internal logic, Port80 diagnostic interface
  - realized as an LPC target
    - supports IO access
- Clock Generator
  - Derivate internal needed clocks and timing pulses from 50MHz CPLD base clock
- Watchdog
  - Watchdog function can cause system reset
  - It can be called by writing value to registers from the LPC interface
- Port 80 Diag
  - POST LED control
- LED
  - Indicates the current state of the system
- Register interface
  - contains all control and state signals
- Synchronizer and Debouncer
  - Synchronizes all external signals into CPLD clock domain
  - Debounces all input from switches and jumpers with mechanical contacts

- Power Sequencing and Platform Control
  - generates the right power up and down sequencing
  - monitors power supplies and disable power supplies if needed
  - generate reset signals
- BIOS CS SWTICH
  - Switch to backup BIOS when major BIOS crash

C.3 FPGA I/O Registers

The Advantech MIC-3332 FPGA communicates with main I/O spaces. The LPC unit is used to interconnect the Intel CM236 LPC signals. This chapter will list down all registers with a short description off the register interface. A detailed explanation can be found in the regarding function block description.

Table C.1: Register Map						
Reg-Nr.:		Mnemonic	R/W LPC	default Ox	Function	LPC Address Ox
0	0	FPGA Vandor ID	RO	13	FPGA Vandor ID[15:8]	440
1	1	FPGA Vandor ID	RO	FE	FPGA Vandor ID[7:0]	441
2	2	OS ShutDown Register	R/W	00	OS ShutDown Flag	442
3	3	Watchdog Count Value	R/W	00	Watchdog Count Value	443
4	4	Watchdog Function	R/W	80	Read for disabling bios switch	444
5	5	FPGA Device ID	RO	33	FPGA Device ID[15:8]	445
6	6	FPGA Device ID	RO	32	FPGA Device[7:0]	446
7	7	Revision ID	RO	00	Revision ID[15:8]	447
8	8	Revision ID	RO	01	Revision ID[7:0]	448
9	9	Power Status	RO	00	Power Status	449
10	A	GA Status	RO	00	GA Status	44a
11	B	GPIO Input Status	RO	00	GPIO Input Status	44b
12	C	GPIO Output Value	R/W	00	GPIO Output Value	44c
13	D	GPIO Output Enable	R/W	00	GPIO Output Value	44d
14	E	Port 80 Status	RO	00	Port 80 Status	44e
15	F	Dual BIOS Switch Register	R/W	00	Dual BIOS Switch	44f

Register Address: IO address 440h-441h
Register Name: FPGA Vandor ID Register
Default Value: 13FE
Attribute: Read Only

Bit	Description	Access
15-0	Vandor ID This field identifies the particular device. This is a 16-bit value assigned to Advantech Co., Ltd.	RO

Register Address: IO address 442h
Register Name: OS ShutDown Flag Register
Default Value: 00
Attribute: Read/Write

Bit	Description	Access
7-1	Reserved	RO
0	0: OS ShutDown disable 1: OS ShutDown enable	RW

Note: This register just for BIOS to write.For customer, please don't use this register.

Register Address: IO address 443h
Register Name: Watchdog Count Value
Default Value: 00
Attribute: Read/Write

Bit	Description	Access
7-0	Watchdog Count Value (default unit:sec)	RW

Register Address: IO address 444h
Register Name: Watchdog Function
Default Value: 80
Attribute: Read/Write

Bit	Description	Access
7	1: dual BIOS enable (default) 0: dual BIOS disable	RO
6:3	Reserved	RW
2:1	00: unit:sec(default) 01: unit:min 10: unit:hour 11:unit:day	RW
0	1: Watchdog Enable 0: Watchdog Disable (default)	RW

Register Address: IO address 445h-446h
Register Name: Device ID
Default Value: 3332
Attribute: Read Only

Bit	Description	Access
15-0	Device ID This field identifies the particular device. This identifier is allocated by the CPLD design team.	RO

Register Address: IO address 447h-448h
Register Name: Revision ID Register
Default Value: 0014
Attribute: Read Only

Bit	Description	Access
0-15	Revision ID Revision changes announcing design changes and additions with impact to the CPLD related firmware and application.	RO

Register Address: IO address 449h

Register Name: Power Status

Default Value: ----

Attribute: Read Only

Bit	Description	Access
0	HANDEL# status	RO
1	J1 ENUM status	RO
2	BD_SEL# status	RO
3	System PLTRST# status	RO
4	PM_ICH_PWROK status	RO
5	System S3# status	RO
6	System S4# status	RO
7	System S5# status	RO

Register Address: IO address 44Ah

Register Name: GA Status

Default Value: 00

Attribute: Read Only

Bit	Description	Access
4-0	GA status	RO
7:5	RSVD	RO

Register Address: IO address 44Bh

Register Name: GPIO Input Status

Default Value: 00

Attribute: Read Only

Bit	Description	Access
7-0	GPIO[7:0] Input Status , RSVD	RO

Note: GPIO setting is reserved, not open.

Register Address: IO address 44Ch

Register Name: GPIO Output Value

Default Value: 00

Attribute: Read/Write

Bit	Description	Access
7-0	GPIO[7:0] Output Value, RSVD	R/W

Note: GPIO setting is reserved, not open.

Register Address: IO address 44Dh

Register Name: GPIO Output Enable

Default Value: 00

Attribute: Read/Write

Bit	Description	Access
7-0	GPIO[7:0] Output Enable, RSVD	R/W

Note: GPIO setting is reserved.

Register Address: IO Address 44Eh

Register Name: IO Port 80 Status

Default Value: --

Attribute: Read Only

Bit	Description	Access
7:0	IO Port 80 status	RO

Register Address: IO Address 44Fh

Register Name: Dual BIOS Switch Register

Default Value: 00

Attribute: Read /Write

Bit	Description	Access
7:0	Dual BIOS Switch 00: Boot from BIOS1 01: Boot from BIOS2 Bit7-Manual Control Other reserved Example: want to change flash BIOS1?need to set this register to 0x80; If want to change flash BIOS2?need to set this register to 0x81.	RW

C.4 CPLD Upgrade

The CPLD can be update via JTAG interface.

C.4.1 JTAG Interface

Table C.2: JTAG Interface				
Connector pin	Pin num	Type	Name	Description
1	--	Power	VCC	3.3V
2	F6	O	FPGA_TDO	
3	F5	I	FPGA_TDI	JTAG configuration pin
4	G1	I	FPGA_TMS	
5	G2	O	FPGA_TCK	
6	--	Power	GND	GND

The MIC-3332 supports JTAG update via debug pin header and Altra download cable.

Appendix D

Glossary

ACPI	Advanced Configuration and Power Interface
API	Application Programming Interface
BIOS	Basic Input/Output System
CPU	Central Processing Unit
CPCI	CompactPCI
DDR4	Double Data Rate 4
ECC	Error Checking and Correction
FCBGA	Flip Chip BGA
Flash	Flash memory
FPGA	Field Programmable Gate Array
FRU	Field Replaceable Unit
GbE	Gigabit Ethernet
GPIO	General Purpose Input / Output
HDD	Hard Disk Drive
HW	HardWare
I/O	Input/Output
IC	Integrated Circuit
I2C	Inter Integrated Circuit
LPC	Low Pin Count
MAC	Medium Access Control
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
RIO	Rear Input/Output
RS-232	Recommended Standard 232
RTC	Real Time Clock
RTM	Rear Transition Module
SATA	Serial Advanced Technology Attachment
SEL	System Event Log
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
SW	SoftWare
UART	Universal Asynchronus Receiver Transmitter
USB	Universal Serial Bus

Appendix D Glossary

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