

**Full-size MiniPCle
PCIe/NVMe SSD 710
Datasheet
(SQF-CMSxx-xG-E8x)**

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Revision History

Rev.	Date	History
0.1	2018/3/9	1. Preliminary release
0.2	2018/6/21	1. Add performance result
0.3	2018/10/21	1. Add operation temperature information
0.4	2019/7/4	1. Updated performance information

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1. Overview

Advantech SQFlash 710 series Full-size MiniPCIe PCIe/NVMe SSD (Solid State Drive) delivers all the advantages of flash disk technology with PCIe Gen3 x2 interface, including being compliant with Full-size MiniPCIe form factor. The device offers a wide range of capacities up to 1TB and its performance can reach up to 1600 MB/s (for read) and 1000 MB/s (for write) based on Toshiba 3D NAND (BiCS3) flash. The lower power consumption makes it an ideal storage choice for high performance demanding mobile devices.

2. Features

■ PCIe Interface

- Compliant with NVMe1.2
- PCI Express Base 3.1
- PCIe Gen 3 x 2 lane & backward compatible to PCIe Gen 2 and Gen 1
- Support up to QD 128 with queue depth of up to 64K
- Support power management

■ Operating Voltage : 3.3V

■ Support StrongECCTM (SECC) of ECC algorithm

■ Support SMART and TRIM commands

■ Temperature Ranges

- Commercial Temperature
 - 0°C to 70°C for operating¹
 - -40°C to 85°C for storage
- Industrial Temperature
 - -40°C to 85°C for operating
 - -40°C to 85°C for storage

*Note : 1. Based on SMART Attribute (Byte index [2 :1] of PCIe-SIG standard, which measured by thermal sensor

■ Mechanical Specification

- Shock : 1,500G / 0.5ms
- Vibration : 20G / 80~2,000Hz

■ Humidity

- Humidity : 5% ~ 95% under 55°C

■ Acquired RoHS 、 WHQL 、 CE 、 FCC Certificate

■ Acoustic : 0 dB

■ Dimension : 50.80 mm x 29.85 mm x 4.75 mm

3. Specification Table

■ Performance

		Sequential Performance (MB/sec)		Random Performance (IOPS @4K)	
		Read	Write	Read	Write
3D NAND (BiCS3)	64 GB	717.50	237.20	16,630	43,008
	128 GB	1,422.00	469.00	37,999	89,602
	256 GB	1,582.00	1,015.00	97,289	117,764
	512 GB	1,570.30	982.70	94,722	117,860
	1 TB	1,564.00	1,010.00	102,449	153,632

NOTES:

1. Based on SQF-CMS 710 series under ambient temperature.
2. Use CrystalDiskMark 5.1.2 with the setting of 1000MB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5]
3. Power Consumption may differ according to flash configuration and platform.
4. The measured power voltage is 3.3V.
5. The performance number is based on 2-channel of PCIe signal are presented in the mPCIe socket. If only 1-channel of PCIe signal is presented then the performance will be reduced by half.

Endurance

JEDEC defined an endurance rating TBW (TeraByte Written), following by the equation below, for indicating the number of terabytes a SSD can be written which is a measurement of SSDs' expected lifespan, represents the amount of data written to the device.

$$\text{TBW} = [(\text{NAND Endurance}) \times (\text{SSD Capacity})] / \text{WAF}$$

- **NAND Endurance:** Program / Erase cycle of a NAND flash.
 - SLC: 100,000 cycles
 - Ultra MLC: 30,000 cycles
 - MLC: 3,000 cycles
 - 3D NAND (BiCS): 3,000 cycles
- **SSD Capacity:** SSD physical capacity in total of a SSD.
- **WAF:** Write Amplification Factor (WAF), as the equation shown below, is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near to 1, guarantees better endurance and lower frequency of data written to flash memory.

$$\text{WAF} = (\text{Lifetime write to flash}) / (\text{Lifetime write to host})$$

Endurance measurement is based on JEDEC 218A/219A client workload and verified with following workload conditions,

- PreCond%full = 100%
 - Trim commands enabled
 - Random data pattern.
- **SQFlash 710 Full-size MiniPCle TBW**

	WAF	TBW
		3D NAND (BiCS3)
64 GB	3.72	52
128 GB	2.52	152
256 GB	2.78	276
512 GB	2.59	593
1 TB	2.22	1383

4. General Description

■ Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, SQF-CMS 710 applies the StrongECCTM (SECC) algorithm, which can detect and correct data errors to ensure data being read correctly, and protects data from corruption.

■ Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, when flash media is not used evenly, some blocks get updated more frequently than others and the lifetime of device would be reduced significantly. Thus, wear leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

Phison provides advanced wear leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static wear leveling algorithms, the life expectancy of the NAND flash is greatly improved.

■ Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Phison implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

■ Power Loss Protection: Flush Manager

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, SQFlash SSD applies the Flush Manager technology, only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

In addition, it is critical for a controller to shorten the time the in-flight data stays in the controller internal cache. Thus, SQFlash applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. With Flush Manager, incoming data would only have a “pit stop” in the cache and then move to NAND flash directly. Also, the onboard DDR will be treated as an “organizer” to consolidate incoming data into groups before written into the flash to improve write amplification.

■ TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD so that blocks of data that are no longer in use can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks at all time.

■ SMART

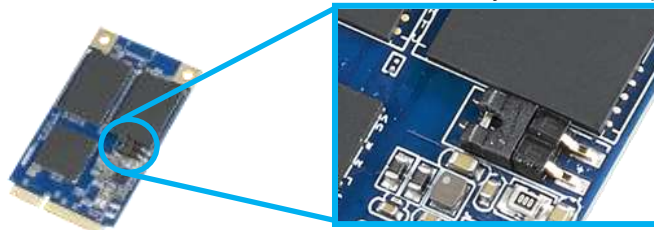
SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a solid state drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users impending failures while there is still time to perform proactive actions, such as save data to another device.

■ Over-Provision

Over Provisioning refers to the preserving additional area beyond user capacity in a SSD, which is not visible to users and cannot be used by them. However, it allows a SSD controller to utilize additional space for better performance and WAF. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

■ Hardware Write Protect Pin

A 2-pin header is mounted and connected to controller reserved GPIO for the drive write protection. When the pins are opened, all of the write command will be carried to a buffer area without real programming to the Flash IC. So the data won't be saved in this mode and will be totally discarded upon power shutting down.



On-board GPIO for Write Protection

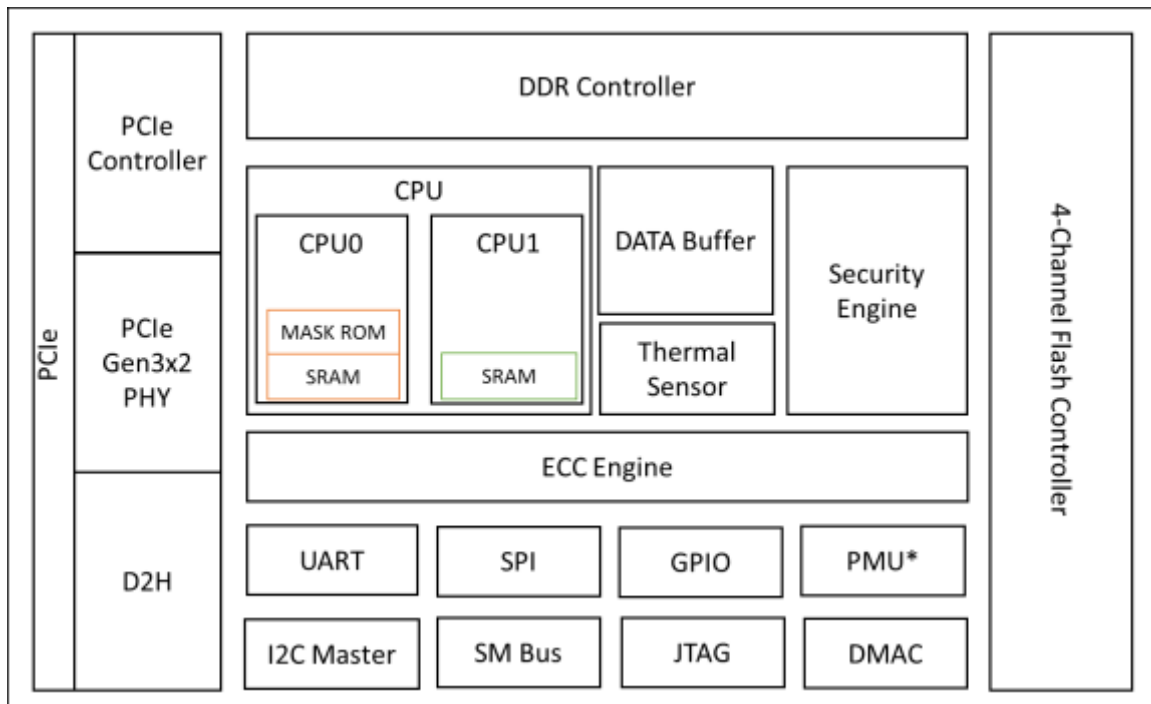
■ Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. Thermal Throttling function is for protecting the drive and reducing the possibility of read / write error due to overheat. The temperature is monitored by the thermal sensor. As the operating temperature continues to increase to threshold temperature, the Thermal Throttling mechanism is activated. At this time, the performance of the drive will be significantly decreased to avoid continuous heating. When the operating temperature falls below threshold temperature, the drive can resume to normal operation.

■ Advanced Device Security Features

- Secure Erase
Secure Erase is a standard NVMe format command and will write all "0xFF" to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings.
- Write Protect
Secure Erase is a standard NVMe format command and will write all "0xFF" to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings.

■ Block Diagram



■ LBA value

Density	LBA
64 GB	125,045,424
128 GB	250,069,680
256 GB	500,118,192
512 GB	1,000,215,216
1 TB	2,000,409,264

5. Pin Assignment and Description

Below table defines the signal assignment of the connector for SSD usage, described in the PCI Express Specification version 1.0 of the PCI-SIG.

PIN#	Name	PIN#	Name
51	NC	52	+3.3Vaux
49	DAS	50	GND
47	UART_RX	48	NC
45	UART_TX	46	NC
43	GND	44	NC
41	+3.3Vaux	42	NC
39	+3.3Vaux	40	GND
37	GND	38	NC
35	GND	36	NC
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	NC
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	PETp1	20	NC
17	PETn1	18	GND
Mechanical Key			
15	GND	16	NC
13	REFCLK+	14	NC
11	REFCLK-	12	GPIO_Erase_3.3V
9	GND	10	GPIO_WP_3.3V
7	CLKREQ#	8	NC
5	PERp1	6	NC
3	PERn1	4	GND
1	PCIE_WAKE	2	NC

6. NVMe Command List

■ Admin commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download
NVM Command Set Specific	
80h	Format NVM
81h	Security Send
82h	Security Receive

■ NVM commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
08h	Write Zeroes
09h	Dataset Management

7. Identify Device Data

The Identify Device Data enables Host to receive parameter information from the device. The parameter words in the buffer have the arrangement and meanings defined in below table. All reserve bits or words are zero

■ Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	SN
63:24	M	Model Number (MN)	Model Number
71:64	M	Firmware Revision (FR)	FW Name
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	0
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0000
83:80	M	Version (VER)	0x00010200
87:84	M	RTD3 Resume Latency (RTD3R)	0x00124F80
91:88	M	RTD3 Entry Latency (RTD3E)	0x0016E360
95:92	M	Optional Asynchronous Events Supported (OAES)	0
239:96	-	Reserved	0
255:240	-	Refer to the NVMe Management Interface Specification for definition	0
257:256	M	Optional Admin Command Support (OACS)	0x0007
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x02
261	M	Log Page Attributes (LPA)	0x03
262	M	Error Log Page Entries (ELPE)	0x3F
263	M	Number of Power States Support (NPSS)	0x04
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x0157
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0193
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0000
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0
295:280	O	Total NVM Capacity (TNVMCAP)	0
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0
315:312	O	Replay Protected Memory Block Support (RPMBS)	0
511:316	-	Reserved	0
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	-	Reserved	0
519:516	M	Number of Namespaces (NN)	0x01
521:520	M	Optional NVM Command Support (ONCS)	0x001E
523:522	M	Fused Operation Support (FUSES)	0
524	M	Format NVM Attributes (FNA)	0
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	0x00FF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x00
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0

Specifications subject to change without notice, contact your sales representatives for the most update information.

533:532	O	Atomic Compare & Write Unit (ACWU)	0x00
535:534	M	Reserved	0
539:536	O	SGL Support (SGLS)	0x00
703:540	M	Reserved	0
IO Command Set Attributes			
2047:704	M	Reserved	0
2048:2079	M	Power State 0 Descriptor	PSD0
2111:2080	O	Power State 1 Descriptor	PSD1
2143:2112	O	Power State 2 Descriptor	PSD2
2175:2144	O	Power State 3 Descriptor	PSD3
2207:2176	O	Power State 4 Descriptor	PSD4
...	-	(N/A)	0
3071:3040	O	Power State 31 Descriptor	PSD31
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Vendor Reserved

■ Identify Namespace Data Structure & NVM Command Set Specific

Bytes	Description
7:0	Namespace Size (NSZE)
15:8	Namespace Capacity (NCAP)
23:16	Namespace Utilization (NUSE)
24	Namespace Features (NSFEAT)
25	Number of LBA Formats (NLBAF)
26	Formatted LBA Size (FLBAS)
27	Metadata Capabilities (MC)
28	End-to-end Data Protection Capabilities (DPC)
29	End-to-end Data Protection Type Settings (DPS)
30	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	Reservation Capabilities (RESCAP)
119:32	Reserved
127:120	IEEE Extended Unique Identifier (EUI64)
131:128	LBA Format 0 Support (LBAF0)
135:132	LBA Format 1 Support (LBAF1)
139:136	LBA Format 2 Support (LBAF2)
143:140	LBA Format 3 Support (LBAF3)
147:144	LBA Format 4 Support (LBAF4)
151:148	LBA Format 5 Support (LBAF5)
155:152	LBA Format 6 Support (LBAF6)
159:156	LBA Format 7 Support (LBAF7)
163:160	LBA Format 8 Support (LBAF8)
167:164	LBA Format 9 Support (LBAF9)
171:168	LBA Format 10 Support (LBAF10)
175:172	LBA Format 11 Support (LBAF11)
179:176	LBA Format 12 Support (LBAF12)
183:180	LBA Format 13 Support (LBAF13)
187:184	LBA Format 14 Support (LBAF14)
191:188	LBA Format 15 Support (LBAF15)
383:192	Reserved
4095:384	Vendor Specific (VS)

■ List of Device Identification for Each Capacity

Capacity	Byte[7:0]: Namespace Size (NSZE)
128 GB	EE7C2B0
256 GB	1DCF32B0
512 GB	3B9E12B0
1 TB	773BD2B0

8. SMART Attributes

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1
[203:202]	2	Temperature Sensor 2
[205:204]	2	Temperature Sensor 3
[207:206]	2	Temperature Sensor 4

9. System Power Consumption

■ Supply Voltage

Parameter	Rating
Operating Voltage	3.3V

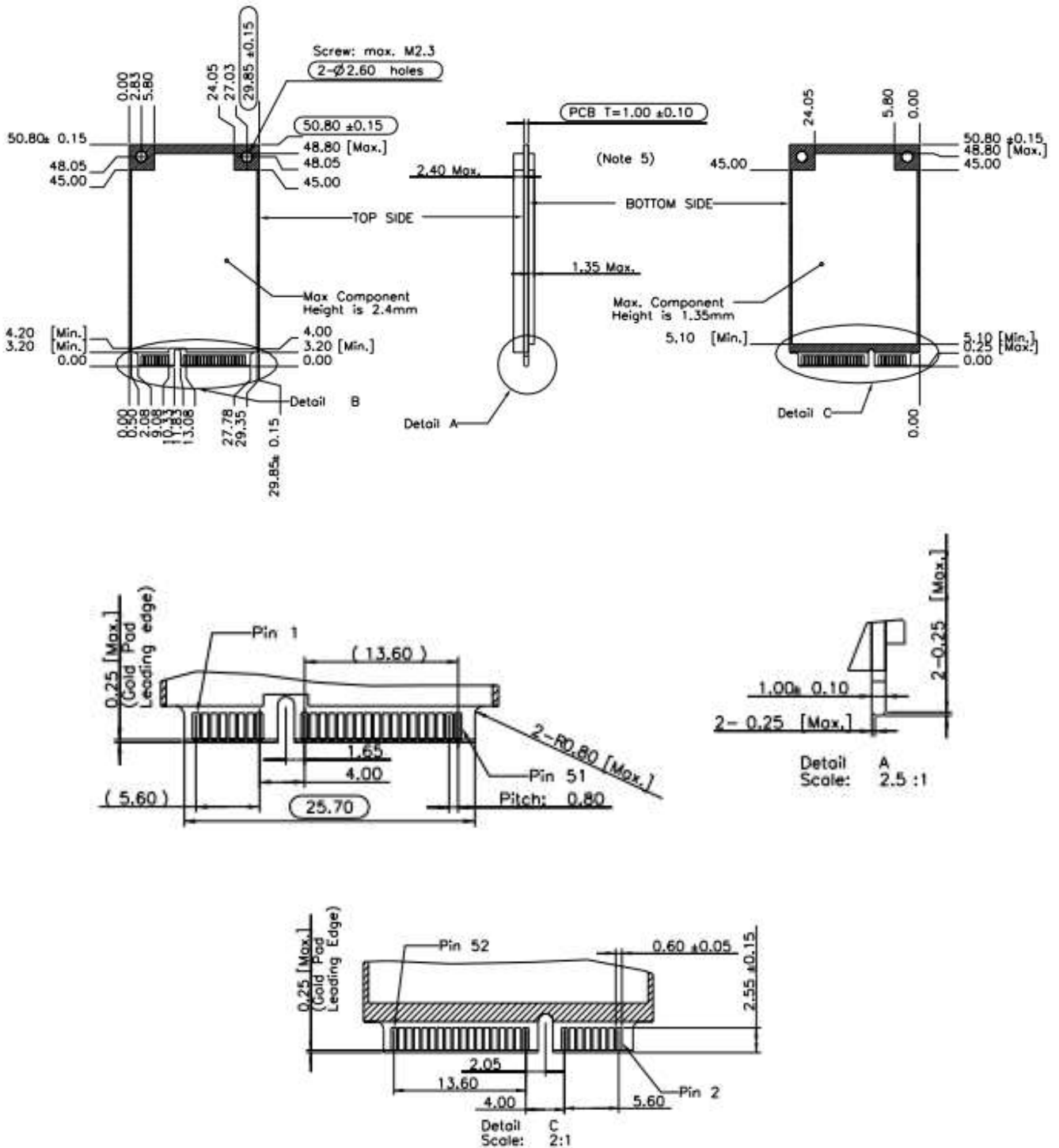
■ Power Consumption

mW		Read	Write	Idle
3D NAND (BiCS3)	64 GB	1,732	1,433	24.8
	128 GB	2,422	1,780	26.7
	256 GB	2,619	2,294	27.4
	512 GB	2,951	2,575	26.4
	1 TB	3,119	2,729	27.1

1. Based on SQF-CMS 710 series under ambient temperature.
2. Use CrystalDiskMark 5.1.2 with the setting of 1000MB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5]
3. Power Consumption may differ according to flash configuration and platform.
4. The measured power voltage is 3.3V.

10. Physical Dimension

Full-size MiniPCIe PCIe/NVMe SSD (Unit: mm)



Appendix: Part Number Table

3D NAND (BiCS3)

Product	Advantech PN
SQF 710 PCIe/NVMe Full-size MiniPCIe 64G 3D NAND (BiCS3) (0~70°C)	SQF-CMSV1-64G-E8C
SQF 710 PCIe/NVMe Full-size MiniPCIe 128G 3D NAND (BiCS3) (0~70°C)	SQF-CMSV2-128G-E8C
SQF 710 PCIe/NVMe Full-size MiniPCIe 256G 3D NAND (BiCS3) (0~70°C)	SQF-CMSV4-256G-E8C
SQF 710 PCIe/NVMe Full-size MiniPCIe 512G 3D NAND (BiCS3) (0~70°C)	SQF-CMSV4-512G-E8C
SQF 710 PCIe/NVMe Full-size MiniPCIe 1T 3D NAND (BiCS3) (0~70°C)	SQF-CMSV4-1T-E8C
SQF 710 PCIe/NVMe Full-size MiniPCIe 64G 3D NAND (BiCS3) (-40~85°C)	SQF-CMSV1-64G-E8E
SQF 710 PCIe/NVMe Full-size MiniPCIe 128G 3D NAND (BiCS3) (-40~85°C)	SQF-CMSV2-128G-E8E
SQF 710 PCIe/NVMe Full-size MiniPCIe 256G 3D NAND (BiCS3) (-40~85°C)	SQF-CMSV4-256G-E8E
SQF 710 PCIe/NVMe Full-size MiniPCIe 512G 3D NAND (BiCS3) (-40~85°C)	SQF-CMSV4-512G-E8E
SQF 710 PCIe/NVMe Full-size MiniPCIe 1T 3D NAND (BiCS3) (-40~85°C)	SQF-CMSV4-1T-E8E