

USER'S MANUAL

MANO560 Series

**Intel® Socket 1700 Core™ i9/ i7/ i5/ i3
Processors Mini ITX Motherboard**

User's Manual



www.axiomtek.com

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CAUTION

If you replace wrong batteries, it causes the danger of explosion. It is recommended by the manufacturer that you follow the manufacturer's instructions to only replace the same or equivalent type of battery and dispose of used ones.

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ESD Precautions

Computer boards have integrated circuits sensitive to static electricity. To prevent chipsets from electrostatic discharge damage, please take care of the following jobs with precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before holding the board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. It discharges static electricity from your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

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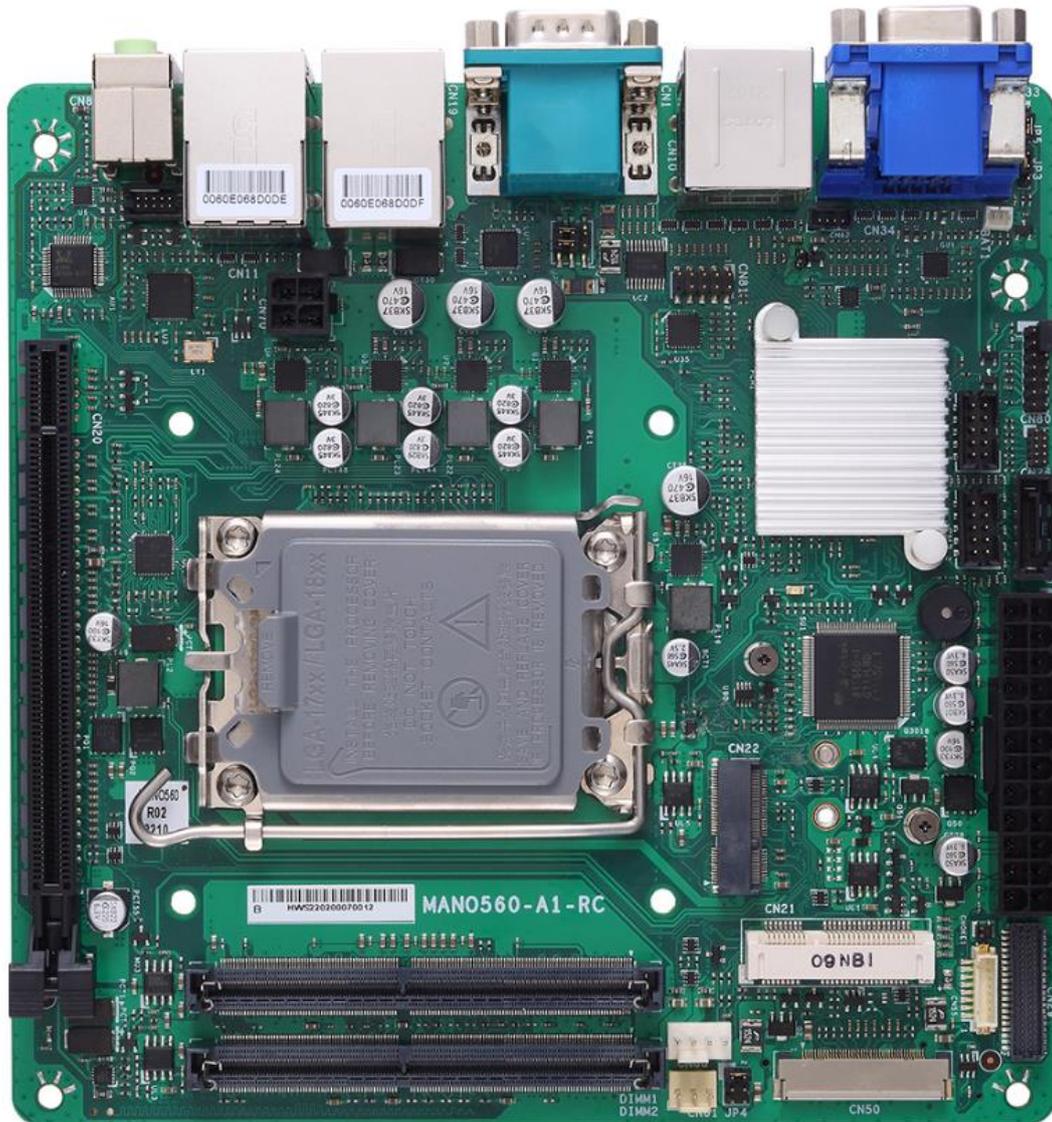
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Section 1

Introduction



The MANO560 Mini-ITX motherboard supports the new 14nm 12th Generation Intel® Core™ i9 / i7/ i5 / i3 and Pentium® processors in LGA1700 package. Featuring the new Intel® H610 Express chipset with two DDR4 3200MHz memory support, this motherboard is built to perform best stability and reliability for industrial applications.

It comes with one SATA 3.0, two USB 3.2 GEN1, five USB 2.0 and four serial ports (one RS-232/422/485, three RS-232) providing robust storage and I/O options. Users also can increase board functionality with PCI-Express x16 and full type PCI-Express Mini Card slot. The high quality MANO560 allows five display interfaces via VGA, HDMI, DisplayPort, LVDS and eDP in quadruplicate views, making it an ideal solution for gaming, workstation, digital signage, medical and other IoT&M2M applications.

1.1 Features

- LGA1700 Socket for 12th Generation Intel® Core™ i9/ i7/ i5/ i3 and Pentium® processors (Alder Lake)
- 2 DDR4 3200MHz memory with maximum capacity up to 64 GB
- 1 PCI-Express x16
- 1 M.2 Key E with size 22x30
- 1 full type PCI-Express Mini Card
- 1 M.2 key B type 2242/3042/3052
- 1 SATA-600
- 2 USB 3.2 GEN1 and 5 USB 2.0

1.2 Specifications

- **CPU**
 - Intel® Alder Lake for LGA1700 Socket CPU (Max TDP at 65W).
- **Chipset**
 - Intel® H610.
- **BIOS**
 - AMI BIOS via SPI interface.
- **System Memory**
 - Two 260-pin SO-DIMM sockets.
 - Maximum up to 64GB DDR4 memory.
 - Support 3200MHz.
- **Onboard Multi I/O**
 - Four serial ports:
 - COM1~COM2 in 9-pin D-Sub (on the rear I/O). Only COM1 supports RS-232/422/485.
 - COM3~COM4 in 2x5-pin header (internal).
- **USB Interface**
 - Two USB 3.2 GEN1 ports (on the rear I/O).
 - Four USB 2.0 ports (on the rear I/O).
 - One 4-pin USB 2.0 wafer for Touch (internal).
- **Ethernet**
 - LAN1: 1000/100/10Mbps Gigabit/Fast Ethernet supports Wake-on-LAN, PXE with Intel® i219V.
 - LAN2: 2500/1000/100/10Mbps Gigabit/Fast Ethernet supports Wake-on-LAN, PXE with Intel® i225V.
- **Serial ATA**
 - One SATA 3.0 port (6Gb/s).
- **Audio**
 - Realtek Codec ALC897.
 - Support line-out/MIC-in (on the rear I/O).
 - Support Line-in/Line-out/Speaker in box header (internal).
- **Display**
 - Intel® Integrated Graphics:
 - One DisplayPort1.3 connector combo with dual USB 3.2 GEN1 connector, support resolution 5120x2880 @60Hz.

- One HDMI1.4 connector, resolution up to 4096x2160 @24Hz.
- One VGA 15-pin D-Sub connector.
- One 24-bit dual channel LVDS and one 8-pin inverter connector. LVDS resolution is max. up to 1920x1200.
- One Embedded DisplayPort (eDP) with resolution max. up to 4096x2304 @60Hz; co-layout with LVDS.
- **Expansion Interface**
 - One PCI-Express x16 slot.
 - One PCI-Express Mini Card.
 - One SIM card slot co-lay with miniPCIe and M.2 Key B socket.
 - One M.2 Key B type 2242/3042/3052 includes PCIe x2, PCIe + SATA3.0, PCIe + USB 3.2 GEN1 interfaces by BOM option. Default is PCIe + SATA3.0.
 - One M.2 Key E type 2230 with PCIe x1 and USB2.0.
- **Power Input**
 - One 24-pin ATX power input connector.
 - One 4-pin ATX v-core power input connector.
- **Operating Temperature**
 - 0°C ~ 60°C.
- **Storage Temperature**
 - -10°C ~ 70°C.
- **Form Factor**
 - Mini ITX (6.7" x 6.7", 17.0cm x 17.0cm).



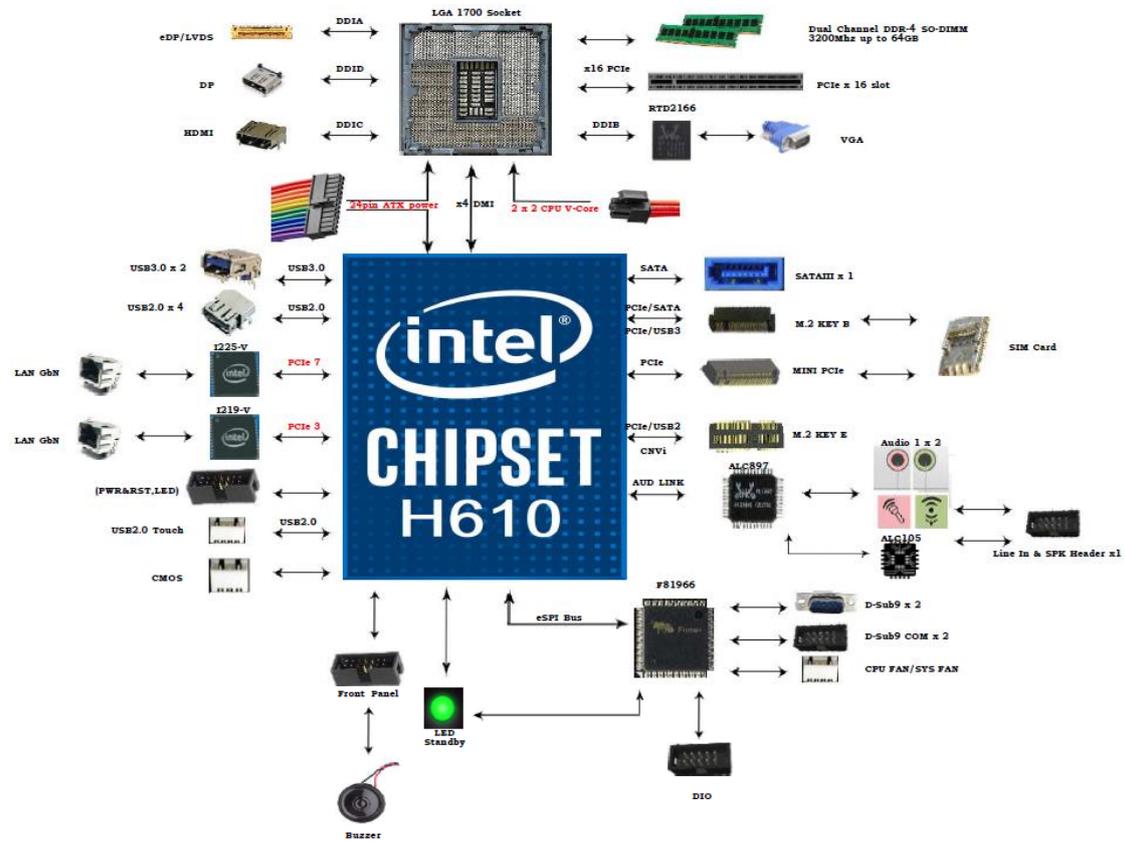
Note

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1.3 Utilities Supported

- Chipset driver
- Graphics driver
- Intel ME driver
- Ethernet driver
- Audio driver
- Serial IO driver

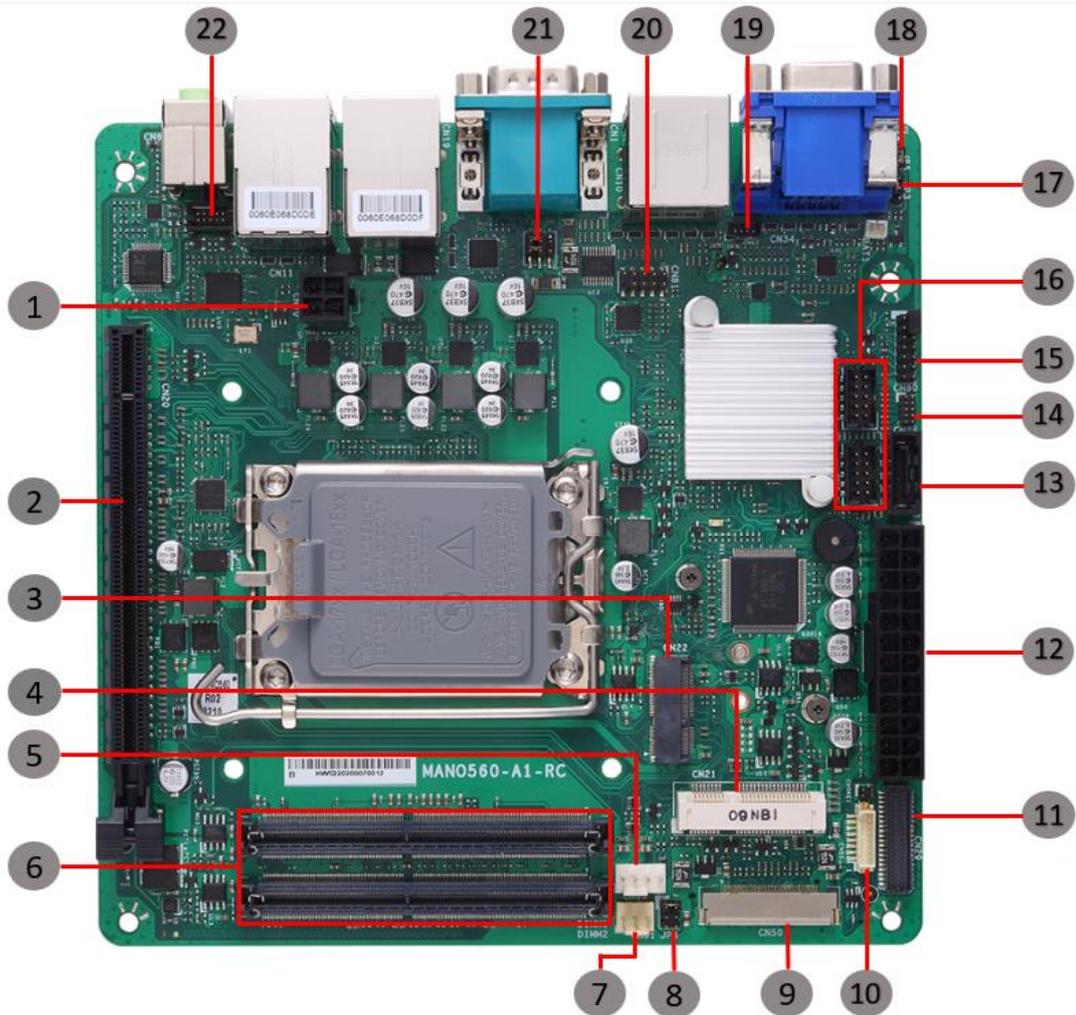
1.4 Block Diagram



Section 2

Board and Pin Assignments

2.1 Board Layout

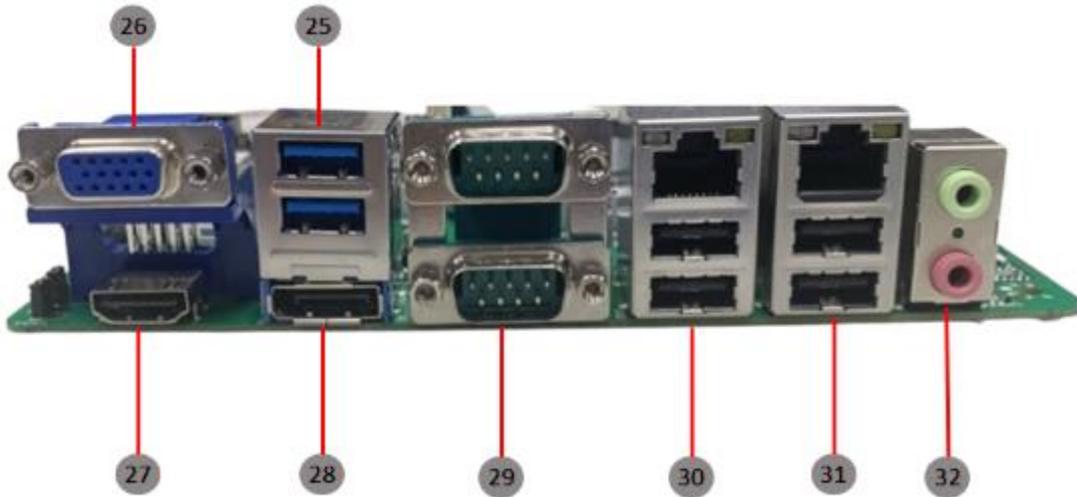


Top View



Bottom View

2.2 Rear I/O



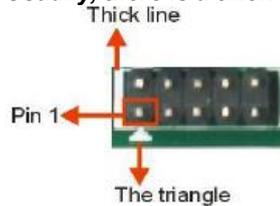
Jumpers/Headers/Connectors			
1	4-pin ATX Power Input Connector (CN70)	17	Clear CMOS (JP3)
2	PCI-Express x16 Slot (CN20)	18	AT/ATX Power Mode Select Jumper (JP5)
3	M.2 Key E Socket (CN22)	19	USB 2.0 Header (CN62)
4	PCI-Express Mini Card Connector (CN21)	20	SPI Header (CN81)
5	CPU Fan Header (CN60)	21	COM VDD Select Jumper (JP1)
6	DDR4 SO-DIMM Connectors (DIMM1, DIMM2)	22	Audio Header (CN52)
7	System Fan Header (CN61)	23	SIM Card Slot (SCN2)
8	LVDS VDD Select Jumper (JP4)	24	M.2 Key B Socket (SCN1)
9	eDP Connector (CN50)	25	USB 3.2 GEN1 Stack Port (CN10)
10	LVDS Backlight Control Header (CN55)	26	VGA Connector (CN34)
11	LVDS Signal Header (CN29)	27	HDMI1.4 Connector (CN33)
12	24-pin ATX Power Input Connector (CN30)	28	DisplayPort1.3 Connector (CN32)
13	SATA 3.0 Connector (CN7)	29	COM1 and COM2 D-Sub Connector (CN1)
14	Digital I/O Connector (CN26)	30	LAN1(RJ-45) and USB 2.0 Connector (CN19)
15	Front Panel Header (CN80)	31	LAN2(RJ-45) and USB 2.0 Connector (CN11)
16	COM3~COM4 Headers (CN3~CN4)	32	Audio Jack (CN82)



Note

To identify the first pin of a header or jumper, please refer to the following information:

- Usually, there is a thick line or a triangle near the header or jumper pin 1.

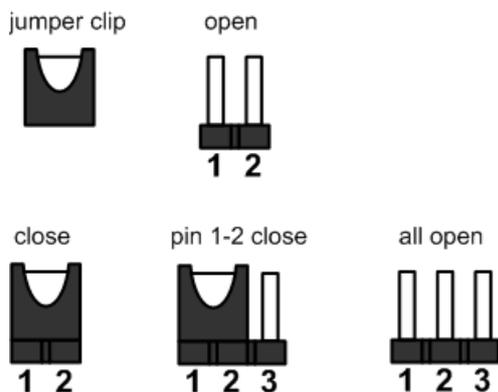


- Square pad, which you can find on the back of the motherboard, is usually used for pin 1.



2.3 Jumper Settings

Jumper is a small component consisting of jumper clip and jumper pins. Install jumper clip on 2 jumper pins to close. And remove jumper clip from 2 jumper pins to open. The following illustration shows how to set up jumper.



Before applying power to MANO560 Series, please make sure all the jumpers are in factory default position. Below you can find a summary table of all jumpers and onboard default settings.



Note

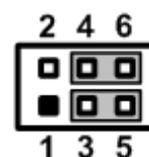
Once the default jumper setting needs to be changed, please do it under power-off condition.

Jumper	Description	Setting
JP1	COM Data/Power Select Default: RS-232 Data	3-5 Close
		4-6 Close
JP3	Clear CMOS Default: Normal Operation	1-2 Close
JP4	LVDS VDD Select Default: +3.3V Level	1-2 Close
JP5	AT/ATX Power Mode Select Default: ATX Mode	1-2 Close

2.3.1 COM1 Data/Power Select (JP1)

This is a 3x2-pin (pitch=2.00mm) jumper. The COM1 port has +5V power capability on DCD and +12V on RI by setting JP1.

Function	Setting
Power: Set COM1 pin 1 to +5V	1-3 close
Data: Set COM1 pin 1 to DCD (Default)	3-5 close
Power: Set COM1 pin 9 to +12V	2-4 close
Data: Set COM1 pin 9 to RI (Default)	4-6 close



2.3.2 Clear CMOS (JP3)

This jumper allows you to clear the Real Time Clock (RTC) RAM in CMOS. You can clear the CMOS memory of date, time, and system setup parameters by erasing the CMOS RTC RAM data. The onboard button cell battery powers the RAM data in CMOS, which includes system setup information such as system passwords.

To erase the RTC RAM:

1. Turn OFF the computer and unplug the power cord.
2. Remove the onboard battery.
3. Move the jumper clip from pins 1-2 (default) to pins 2-3. Keep the clip-on pins 2-3 for about 5~10 seconds, then move the clip back to pins 1-2.
4. Re-install the battery.
5. Plug the power cord and turn ON the computer.
6. Hold down the key during the boot process and enter BIOS setup to re-enter data.

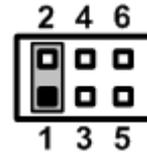
Function	Setting
Normal operation (Default)	1-2 close
Clear CMOS	2-3 close



2.3.3 LVDS VDD Select (JP4)

The motherboard supports voltage selection for flat panel displays. Use this 2x3-pin (pitch=2.0mm) jumper to set up VDD power of the LVDS connector. To prevent hardware damage, before connecting please make sure that the input voltage of LVDS panel is correct.

Function	Setting
+3.3V level (Default)	1-2 close
+5V level	2-4 close
+12V level	5-6 close



2.3.4 AT/ATX Power Mode Select (JP5)

This 3-pin (pitch=2.0mm) jumper allows you to select AT or ATX power mode.

Function	Setting
ATX mode (Default)	1-2 close
AT mode	2-3 close



2.4 Connectors

Signals go to other parts of the system through connectors. Loose or improper connection might cause problems, please make sure all connectors are properly and firmly connected. Here is a summary table showing connectors on the hardware.

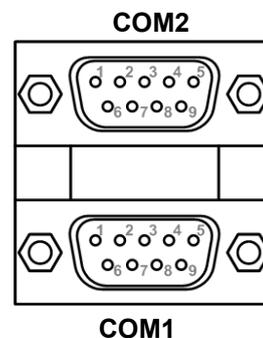
Connector	Description
CN1	COM1 and COM2 D-Sub Connector
CN3~CN4	COM3~COM4 Headers
CN7	SATA 3.0 Connector
CN10	USB 3.2 GEN1 Stack Port
CN11, CN19	LAN and USB 2.0 Connectors
CN20	PCI-Express x16 Slot
CN21	PCI-Express Mini Card Connector
CN22	M.2 Key E Socket
CN26	Digital I/O Connector
CN29	LVDS Signal Header
CN30, CN70	ATX Power Input Connectors
CN32	DisplayPort Connector
CN33	HDMI1.4 Connector
CN34	VGA Connector
CN50	eDP Connector
CN52	Audio Header
CN55	LVDS Backlight Control Header
CN60, CN61	Fan Headers
CN62	USB 2.0 Header
CN80	Front Panel Header
CN81	SPI Header
CN82	Audio Jack
SCN1	M.2 Key B Socket
SCN2	SIM Card Slot

2.4.1 COM1 and COM2 D-Sub Connector (CN1)

The CN1 is a double 9-pin D-Sub connector for COM1 and COM2 serial port interfaces on the rear I/O. Only COM1 supports RS-232/422/485 mode. The pin assignments of RS-232/422/485 are listed in table below.

COM1:

Pin	RS-232 (3T/5R)	RS-422 (1T/1R Full Duplex)	RS-485 (1T/1R TX Enable Low Active)
1	COM1C_DCD ^[*]	TX (-)	(R (-) / T (-))
2	COM1C_RXD	TX (+)	(R (+) / T (+))
3	COM1C_TXD	RX (+)	NC
4	COM1C_DTR	RX (-)	NC
5	GND	GND	GND
6	COM1C_DSR	NC	NC
7	COM1C_RTS	NC	NC
8	COM1C_CTS	NC	NC
9	COM1C_RI ^[*]	NC	NC



Note

^[*]: Pin 1 of COM1 can be DCD/+5V and pin 9 of COM1 can be RI/+12V by selecting JP1 (see section 2.3.1).

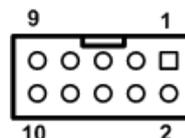
COM2:

Pin	Signal	Pin	Signal
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI		

2.4.2 COM3~COM4 Headers (CN3~CN4)

The motherboard comes with two 2x5-pin (pitch=2.00mm) headers for COM3~COM4 serial port interfaces.

Pin	Signal	Pin	Signal
1	DCD	2	DSR
3	RX	4	RTS
5	TX	6	CTS
7	DTR	8	RI
9	GND	10	NC



2.4.3 SATA 3.0 Connectors (CN7)

This connector supports the thin Serial ATA cable for primary internal storage device.

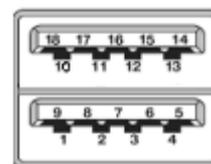
Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND



2.4.4 USB 3.2 GEN1 Stack Port (CN10)

The motherboard comes with one stacked Universal Serial Bus (compliant with USB 3.2 GEN1) connector on the rear I/O for installing USB peripherals such as a keyboard, mouse, scanner, etc.

Pin	Signal	Pin	Signal
1	USB_PWR	10	USB_PWR
2	USB#1_D-	11	USB#2_D-
3	USB#1_D+	12	USB#2_D+
4	GND	13	GND
5	SSRX1-	14	SSRX2-
6	SSRX1+	15	SSRX2+
7	GND	16	GND
8	SSTX1-	17	SSTX2-
9	SSTX1+	18	SSTX2+

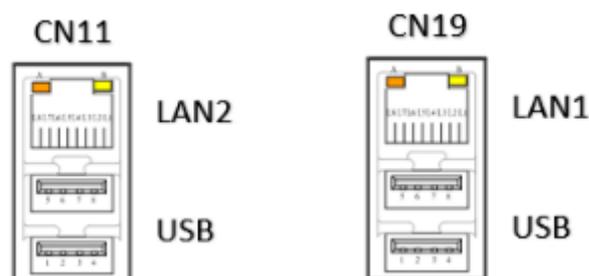


2.4.5 LAN and USB 2.0 Connectors (CN11 and CN19)

The motherboard supports two Ethernet ports (CN11, CN19): two RJ45 connectors with CN11: Intel® i225-V controller support 10/100/1000/2500Mbps. CN19: Intel® i219-V controller support 10/100/1000 Mbps.

The Universal Serial Bus (compliant with USB 2.0) connectors on the rear I/O are for installing USB peripherals such as keyboard, mouse, scanner, etc.

Pin	LAN Signal	Pin	LAN Signal
L1	Tx+ (Data transmission positive)	L2	Tx- (Data transmission negative)
L3	Rx+ (Data reception positive)	L4	RJ-1 (For 1000 Base-T only)
L5	RJ-1 (For 1000 Base-T only)	L6	Rx- (Data reception negative)
L7	RJ-1 (For 1000 Base-T only)	L8	RJ-1 (For 1000 Base-T only)
A	Speed LED LAN1: Intel® i219-V OFF: 10Mbps data rate Green: 100Mbps data rate Orange: 1Gbps data rate LAN2: Intel® i225-V OFF: 10/100Mbps data rate Green: 1Gbps data rate Orange: 2.5Gbps data rate	B	Active LED(Yellow) OFF: No link Blinking: Link established; data activity detected



Note

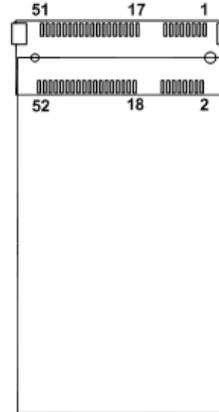
- **CN11/CN19 supports Wake-on-LAN.**

Pin	USB Signal	Pin	USB Signal
1	USB VCC (+5V level)	5	USB VCC (+5V level)
2	USB _D-	6	USB _D-
3	USB _D+	7	USB _D+
4	GND	8	GND

2.4.6 PCI-Express Mini Card Connector (CN21)

The CN21 complies with PCI-Express Mini Card Spec. V1.2.

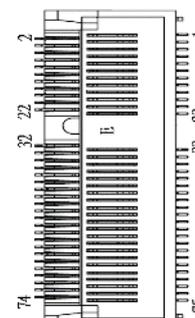
Pin	Signal	Pin	Signal
1	WAKE#	2	+3.3VAUX
3	NC	4	GND
5	NC	6	+1.5V
7	CLKREQ#	8	UIM_PWR/NC
9	GND	10	UIM_DAT/NC
11	REFCLK-	12	UIM_CLK/NC
13	REFCLK+	14	UIM_REST/NC
15	GND	16	UIM_VPP/NC
17	NC	18	GND
19	NC	20	NC
21	GND	22	PERST#
23	PCIE_RX_D-	24	+3.3VAUX
25	PCIE_RX_D+	26	GND
27	GND	28	+1.5V
29	GND	30	SMB_CLK
31	PCIE_TX_D-	32	SMB_DATA
33	PCIE_TX_D+	34	GND
35	GND	36	USB_D-
37	GND	38	USB_D+
39	+3.3VAUX	40	GND
41	+3.3VAUX	42	NC
43	GND	44	NC
45	NC	46	NC
47	NC	48	+1.5V
49	NC	50	GND
51	NC	52	+3.3VAUX



2.4.7 M.2 Key E Socket (CN22)

The motherboard comes with one M.2 Key E socket (PCIe & USB2.0), The CN22 supports CNVi module.

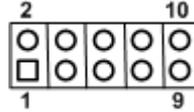
Pin	Signal	Pin	Signal
1	GND	2	+3.3V_SBY
3	USB_D+	4	+3.3V_SBY
5	USB_D-	6	NC
7	GND	8	M.2_BT_PCMCLK
9	CNVI_WGR_DATA1_D-	10	M.2_BT_PCMRST
11	CNVI_WGR_DATA1_D+	12	M.2_BT_PCMMIN
13	GND	14	M.2_BT_PCMOUT
15	CNVI_WGR_DATA0_D-	16	NC
17	CNVI_WGR_DATA0_D+	18	GND
19	GND	20	UART_BT_WAKE-
21	CNVI_WGR_CLK_D-	22	CNVI_BRI_RSP
23	CNVI_WGR_CLK_D+	24	Key E
25	Key E	26	
27		28	
29		30	
31		32	
33	GND	34	CNVI_RGI_RSP
35	PCIE_TX_+	36	CNVI_BRI_DT
37	PCIE_TX_-	38	CL_RST
39	GND	40	CL_DATA
41	PCIE_RX_+	42	CL_CLK
43	PCIE_RX_-	44	CNVI_GNSS_PA_BLANKING
45	GND	46	CNVI_MFUART_TXD
47	CLK_PCIE_+	48	CNVI_MFUART_RXD
49	CLK_PCIE_-	50	SUSCLK (+3.3V Level)
51	GND	52	PERST# (+3.3V Level)
53	CLKREQ0#	54	BT_RF_KILL
55	PEWAKE0#	56	WIFI_RF_KILL
57	GND	58	NC
59	CNVI_WT_DATA1_D-	60	NC
61	CNVI_WT_DATA1_D+	62	NC
63	GND	64	GND
65	CNVI_WT_DATA0_D-	66	NC
67	CNVI_WT_DATA0_D+	68	NC
69	GND	70	NC
71	CNVI_WT_CLK_D-	72	+3.3V_SBY
73	CNVI_WT_CLK_D+	74	+3.3V_SBY
75	GND		



2.4.8 Digital I/O Connector (CN26)

The CN26 is a 2x5-pin (pitch=2.00mm) connector for digital I/O interface.

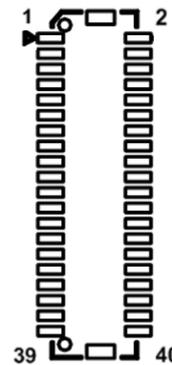
Pin	Signal
1	5V
2	DO0
3	DI0
4	DO1
5	DI1
6	DO2
7	DI2
8	DO3
9	DI3
10	GND



2.4.9 LVDS Signal Connector (CN29)

The CN29 is a 2x20-pin (pitch=1.00mm) connector for LVDS panel interface

Pin	Signal	Pin	Signal
1	VDD ^[*]	2	VDD ^[*]
3	VDD ^[*]	4	VDD ^[*]
5	VDD ^[*]	6	VDD ^[*]
7	LVDS_EDID_SCL	8	LVDS_EDID_SDA
9	GND	10	GND
11	LVDS_B_DATA0-	12	LVDS_B_DATA3-
13	LVDS_B_DATA0+	14	LVDS_B_DATA3+
15	GND	16	GND
17	LVDS_B_DATA1-	18	LVDS_B_CLK-
19	LVDS_B_DATA1+	20	LVDS_B_CLK+
21	GND	22	GND
23	LVDS_B_DATA2-	24	LVDS_A_DATA0-
25	LVDS_B_DATA2+	26	LVDS_A_DATA0+
27	GND	28	GND
29	LVDS_A_DATA3-	30	LVDS_A_DATA1-
31	LVDS_A_DATA3+	32	LVDS_A_DATA1+
33	GND	34	GND
35	LVDS_A_CLK-	36	LVDS_A_DATA2-
37	LVDS_A_CLK+	38	LVDS_A_DATA2+
39	GND ^l	40	GND



Note

^[*]: Panel power VDD is 3.3V by default, 5V or 12V is selectable by jumper JP4, see section 2.3.3.

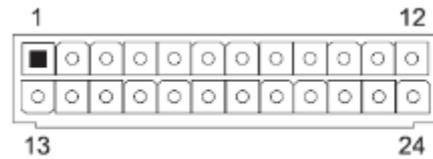
2.4.10 ATX Power Input Connectors (CN30 and CN70)

Steady and sufficient power can be supplied to all components on the board by connecting power connector. Please make sure all components and devices are properly installed before connecting the power connector.

For better compatibility, we recommend using a standard ATX 24-pin and 4-pin power supply for these connectors. External power supply plug fits into the connector in only one orientation. Properly press down power supply plug until it completely and firmly fits into this connector. Loose connection may cause system instability.

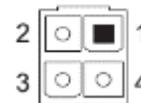
CN30:

Pin	Signal	Pin	Signal
13	3.3V	1	+3.3V
14	-12V	2	+3.3V
15	GND	3	GND
16	PS_ON	4	+5V
17	GND	5	GND
18	GND	6	+5V
19	GND	7	GND
20	NC	8	PW_OK
21	+5V	9	+5VSB
22	+5V	10	+12V
23	+5V	11	+12V
24	GND	12	+3.3V



The CN70 provides +12V to the CPU power circuit.

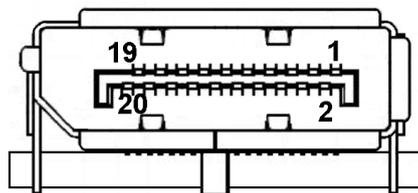
Pin	Signal
1	+12V
2	+12V
3	GND
4	GND



2.4.11 DisplayPort1.3 Connector (CN32)

The motherboard comes with DisplayPort interface on the rear I/O.

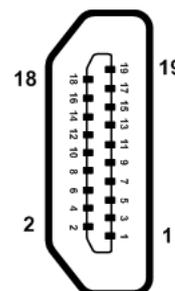
Pin	Signal
1	DP_TX0_+
2	GND
3	DP_TX0_-
4	DP_TX1_+
5	GND
6	DP_TX1_-
7	DP_TX2_+
8	GND
9	DP_TX2_-
10	DP_TX3_+
11	GND
12	DP_TX3_-
13	GND
14	GND
15	DP_AUX+
16	GND
17	DP_AUX-
18	DP_HPD
19	GND
20	+3.3V



2.4.12 HDMI1.4 Connector (CN33)

The HDMI (High-Definition Multimedia Interface) is a compact digital interface which can transmit high-definition video and high-resolution audio over a single cable.

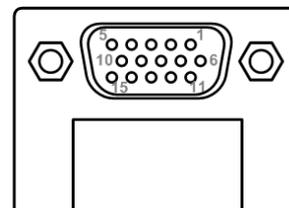
Pin	Signal	Pin	Signal
1	HDMI OUT_DATA2+	2	GND
3	HDMI OUT_DATA2-	4	HDMI OUT_DATA1+
5	GND	6	HDMI OUT_DATA1-
7	HDMI OUT_DATA0+	8	GND
9	HDMI OUT_DATA0-	10	HDMI OUT_CLK+
11	GND	12	HDMI OUT_CLK-
13	NC	14	NC
15	HDMI OUT_SCL	16	HDMI OUT_SDA
17	GND	18	+5V
19	HDMI_HPDET		



2.4.13 VGA Connector (CN34)

The CN34 is a high rise 15-pin D-Sub connector which is commonly used for VGA display. This VGA interface configuration can be configured via software utility.

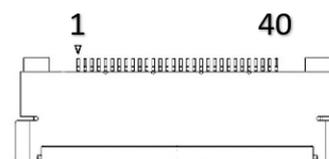
Pin	Signal	Pin	Signal
1	Red	2	Green
3	Blue	4	NC
5	GND	6	GND
7	GND	8	GND
9	VCC	10	GND
11	NC	12	DDC DATA
13	Horizontal Sync	14	Vertical Sync
15	DDC CLK		



2.4.14 eDP Connector (CN50)

This connector supports 18/24 bit single-channel panels.

Pin	Signal	Pin	Signal
1	VDD ^[*]	2	VDD ^[*]
3	VDD ^[*]	4	VDD ^[*]
5	NC	6	GND
7	GND	8	GND
9	GND	10	EMB_HPD
11	GND	12	EDP_TXN3C
13	EDP_TXP3_C	14	GND
15	EDP_TXN2_C	16	EDP_TXP2_C
17	GND	18	EDP_TXN1_C
19	EDP_TXP1_C	20	GND
21	EDP_TXN0_C	22	EDP_TXP0_C
23	GND	24	EMB_AUXP
25	EMB_AUXN	26	GND
27	VSS_EDP_AMOLED	28	VSS_EDP_AMOLED
29	VSS_EDP_AMOLED	30	VSS_EDP_AMOLED
31	NC	32	EDP_BKLTCTL
33	EDP_BKLTEN	34	NC
35	NC	36	VCC_EDP_BKLT
37	VCC_EDP_BKLT	38	VCC_EDP_BKLT
39	VCC_EDP_BKLT	40	NC



Note

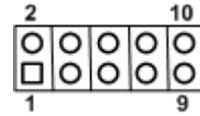
[*]: Panel power VDD is 3.3V by default, 5V or 12V is selectable by jumper JP4, see section 2.3.3.

[**]: CN50 is co-layout with LVDS signal connector (CN29); they can't be accessed simultaneously.

2.4.15 Audio Header (CN52)

The CN52 is a 2x5-pin (pitch=1.27mm) header for convenient connection and control of audio devices.

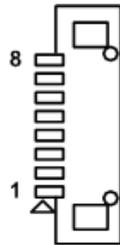
Pin	Signal	Pin	Signal
1	GND	2	GND
3	LINE_IN_L	4	GND
5	LINE_IN_R	6	GND
7	SPKOUT_L	8	GND
9	SPKOUT_R	10	GND



2.4.16 LVDS Backlight Control Header (CN55)

The CN55 is an 8-pin (pitch=1.25mm) header for LVDS backlight control interface.

Pin	Signal
1	+12V
2	+12V
3	+5V
4	LVDS_BKL_EN
5	GND
6	GND
7	GND
8	LVDSPWMOUT

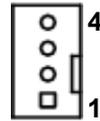


2.4.17 Fan Headers (CN60 and CN61)

The motherboard has two fan headers. The fan cable and connector may be different according to the fan manufacturer. Connect the fan cable to the connector while matching the black wire to pin#1. CN60 and CN61 both support Smart FAN function.

CN60: CPU fan header, 4-pin (pitch=2.54mm)

Pin	Signal
	GND
2	FANPVOUT
3	FAN_TACH
4	FANPWMOUT



CN61: System fan header, 3-pin (pitch=2.54mm)

Pin	Signal
1	GND
2	FANPVOUT
3	FAN_TACH



2.4.18 USB 2.0 Header (CN62)

The CN62 is a 1x4-pin (pitch=1.25mm) header for USB 2.0 interface.

Pin	Signal
1	+5V
2	D+
3	D-
4	GND



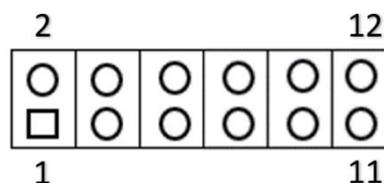
Note

Cable is optional. (Reference part number "594P8802810E")

2.4.19 Front Panel Header (CN80)

The CN80 is a 2x6-pin (pitch=2.54mm) header. It includes Power-on, Reset, HDD LED and Power LED connections, allowing user to connect the PC case's front panel switch functions.

Pin	Signal	Pin	Signal
1	Buzzer	2	Buzzer
3	EXT SPK-	4	EXT SPK+
5	PWRLED-	6	PWRLED+
7	PWRSW-	8	PWRSW+
9	HW RST-	10	HW RST+
11	HDD LED-	12	HDD LED+



Internal Buzzer and External Speaker

Pin 1, 2, 3 and 4 connect the case-mounted speaker unit or internal buzzer. While connecting the board to an internal buzzer, please set pin 1 and 2 closed; while connecting to an external speaker, you need to set pins 1 and 2 opened and connect the speaker cable to pin 3 and pin 4.

Power LED

Pin 5 connects cathode (-) of LED and pin 6 connects anode (+) of LED. The power LED lights up when the system is powered on.

Power On/Off Button

Pin 7 and 8 connect the power button on front panel to the board, which allows users to turn on or off power supply.

System Reset Switch

Pin 9 and 10 connect the case-mounted reset switch that reboots your computer without turning off the power switch. It is a better way to reboot your system for a longer life of system power supply.

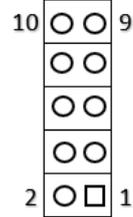
HDD Activity LED

This connection is linked to hard drive activity LED on the control panel. LED flashes when HDD is being accessed. Pin 11 and 12 connect the hard disk drive to the front panel HDD LED, pin 11 is assigned as cathode (-) and pin 12 is assigned as anode (+).

2.4.20 SPI Header (CN81)

The CN81 is a 9-pin (pitch=2.00mm) connector for SPI interface.

Pin	Signal
1	NC
2	WP
3	VCC
4	GND
5	CS
6	CLK
7	MISO
8	MOSI
9	HD



2.4.21 Audio Jack (CN82)

The motherboard provides HD audio jack on the rear I/O. Install audio driver, and then attach audio devices to CN82.

Pin Color	Signal
Green	Line-out
Pink	MIC-in



2.4.22 M.2 Key B Socket (SCN1)

The SCN1 is a M.2 Key B connector. It is suggested to install the M.2 storage module via SATA with 22mm width and 42mm length or the M.2 cellular module via USB 2.0 with 30mm width and 42mm length. It also supports the M.2 storage module via PCIe x2 by BOM option with hardware change.

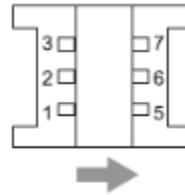
Pin	Signal	Pin	Signal
1	CONFIG_3	2	+3.3V_SBY
3	GND	4	+3.3V_SBY
5	GND	6	Full Card PWR OFF
7	USB_D+	8	NC
9	USB_D-	10	M2_DAS
11	GND	12	Key B
13	Key B	14	
15		16	
17		18	
19		20	
21		CONFIG_0	22
23	NC	24	NC
25	NC	26	NC
27	GND	28	NC
29	PCIE1_RX-/USB3_RX-	30	UIM_RST
31	PCIE1_RX+/USB3_RX+	32	UIM_CLK
33	GND	34	UIM_DATA
35	PCIE1_TX-/USB3_TX-	36	UIM_PWR
37	PCIE1_TX+/USB3_TX+	38	DEVSLP
39	GND	40	NC
41	PCIE0_RX-/SATA1_RX+	42	NC
43	PCIE0_RX+/SATA1_RX-	44	NC
45	GND	46	NC
47	PCIE0_TX-/SATA1_TX-	48	NC
49	PCIE0_TX+/SATA1_RX+	50	PERST#
51	GND	52	CLKREQ#
53	PCIE_CLK_N	54	PEWAKE#
55	PCIE_CLK_P	56	NC
57	GND	58	NC
59	NC	60	NC
61	NC	62	NC
63	NC	64	NC
65	NC	66	SIM_DET
67	M2_WWAN_RST_N	68	SUSCLK
69	CONFIG1	70	+3.3V_DUAL
71	GND	72	+3.3V_DUAL
73	GND	74	+3.3V_DUAL
75	CONFIG2		



2.4.23 SIM Card Slot (SCN2)

The SCN2 is for inserting SIM Card which is mainly used in wireless network application.

Pin	Signal
1	UIM_PWR
2	UIM_RST
3	UIM_CLK
4	N/A
5	GND
6	VPP
7	DATA



Section 3

AMI BIOS Setup Utility

The AMI UEFI BIOS provides users with a built-in setup program to modify basic system configuration. All configured parameters are stored in a flash chip to save the setup information whenever the power is turned off. This chapter provides users with detailed description about how to set up basic system configuration through the AMI BIOS setup utility.

3.1 Starting

To enter the setup screens, follow the steps below:

1. Turn on the computer and press during the Power On Self Test (POST) to enter BIOS setup, otherwise, POST will continue with its test routines.
2. Once you enter the BIOS, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Advanced and Chipset menus.



Note

If your computer cannot boot after making and saving system changes with BIOS setup, you can restore BIOS optimal defaults by pressing F9.

It is strongly recommended that you should avoid changing the chipset's defaults. Both AMI and your system manufacturer have carefully set up these defaults that provide the best performance and reliability.

3.2 Navigation Keys

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F9>, <F10>, <F11>, <F12>, <Enter>, <ESC>, <Arrow> keys, and so on.



Note

Some of the navigation keys differ from one screen to another.

Hot Keys	Description
→← Left/Right	The Left and Right <Arrow> keys allow you to select a setup screen.
↑↓ Up/Down	The Up and Down <Arrow> keys allow you to select a setup screen or sub screen.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub screens.
+– Plus/Minus	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item.
F1	The <F1> key allows you to display the General Help screen.
F9	The <F9> key allows you to Load Optimized Defaults.
F10	The <F10> key allows you to save any changes you have made and exit Setup.
F11	The <F11> key allows you to print the BIOS setting screen.
F12	The <F12> key allows you to update BIOS.
Esc	The <Esc> key allows you to discard any changes you have made and exit the Setup. Press the <Esc> key to exit the setup without saving your changes.

3.3 Main Menu

When you first enter the setup utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. System Time/Date can be set up as described below. The Main BIOS setup screen is shown below.



BIOS Information

Display system BIOS information.

System Language

Use this option to choose the system default language.

System Date/Time

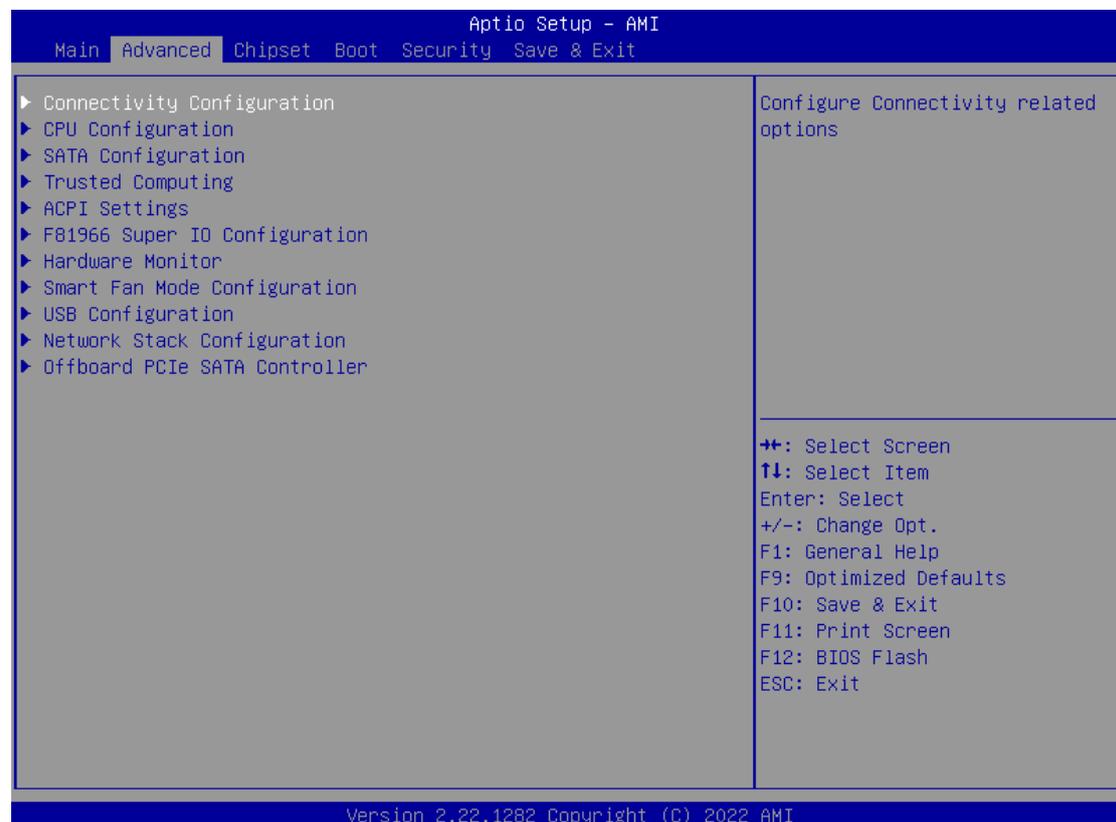
Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

3.4 Advanced Menu

The Advanced menu also allows users to set configuration of the CPU and other system devices. You can select any of the items in the left frame of the screen to go to the sub menus:

- ▶ Connectivity Configuration
- ▶ CPU Configuration
- ▶ SATA Configuration
- ▶ Trusted Computing
- ▶ ACPI Settings
- ▶ F81966 Super IO Configuration
- ▶ Hardware Monitor
- ▶ Smart Fan Mode Configuration
- ▶ USB Configuration
- ▶ Network Stack Configuration
- ▶ Offboard PCIe SATA Controller

For items marked with “▶”, please press <Enter> for more options.



● **Connectivity Configuration**

The CNVi (Connectivity Integration) is a proprietary connectivity interface by Intel for Wi-Fi and Bluetooth radios to lower costs and simplify their wireless modules.



CNVi Mode

This option configures Connectivity.

1. Auto Detection: If Discrete solution is discovered it will be enabled by default.
2. Disable Integrated: Disables Integrated Solution.

RFI Mitigation

This is an option intended to Enable/Disable DDR-RFIM feature for Connectivity.

Preboot BLE

This option is used to enable Preboot Bluetooth function.

WWAN Configuration

Select the M.2 WWAN Device options to enable:

1. Disabled (Default)
2. 4G – 7360/7560 (Intel)
3. 5G – M80 (MediaTek) Modems

- **CPU Configuration**

This screen shows CPU information.



Intel (VMX) Virtualization Technology

Enable or disable Intel Virtualization Technology. When enabled, a VMM (Virtual Machine Mode) can utilize the additional hardware capabilities. It allows a platform to run multiple operating systems and applications independently, hence enabling a single computer system to work as several virtual systems.

Hyper-Threading

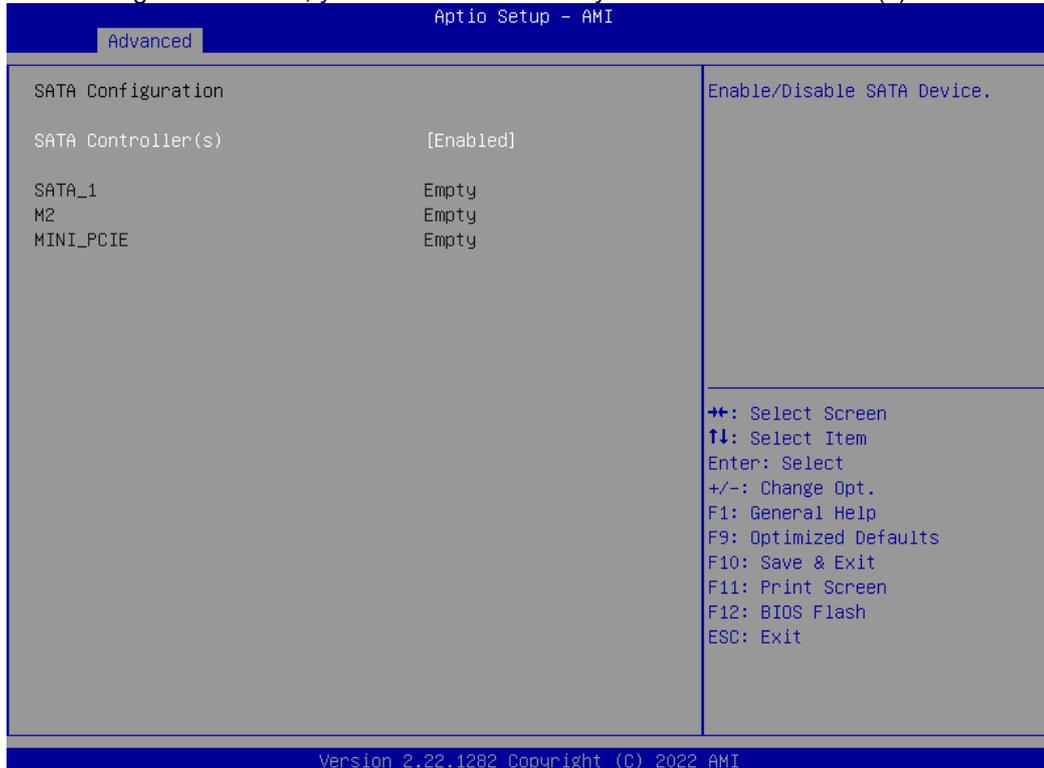
Enable or disable Hyper-Threading Technology. When enabled, it allows a single physical processor to multitask as multiple logical processors. When disabled, only one thread per enabled core is enabled.

Turbo Mode

Enable or disable processor Turbo Mode (requires Intel® Speed Step or Intel® Speed Shift to available and enabled) allowing processor cores to run faster but not exceed CPU defined frequency limits.

- **SATA Configuration**

During system boot up, BIOS automatically detects the presence of SATA devices. In the SATA Configuration menu, you can see all currently installed SATA device(s).



SATA Controller(s)

Enable or disable the SATA Controller feature.

- **Trusted Computing**

This screen provides function for specifying the TPM settings.



TPM Device Selection

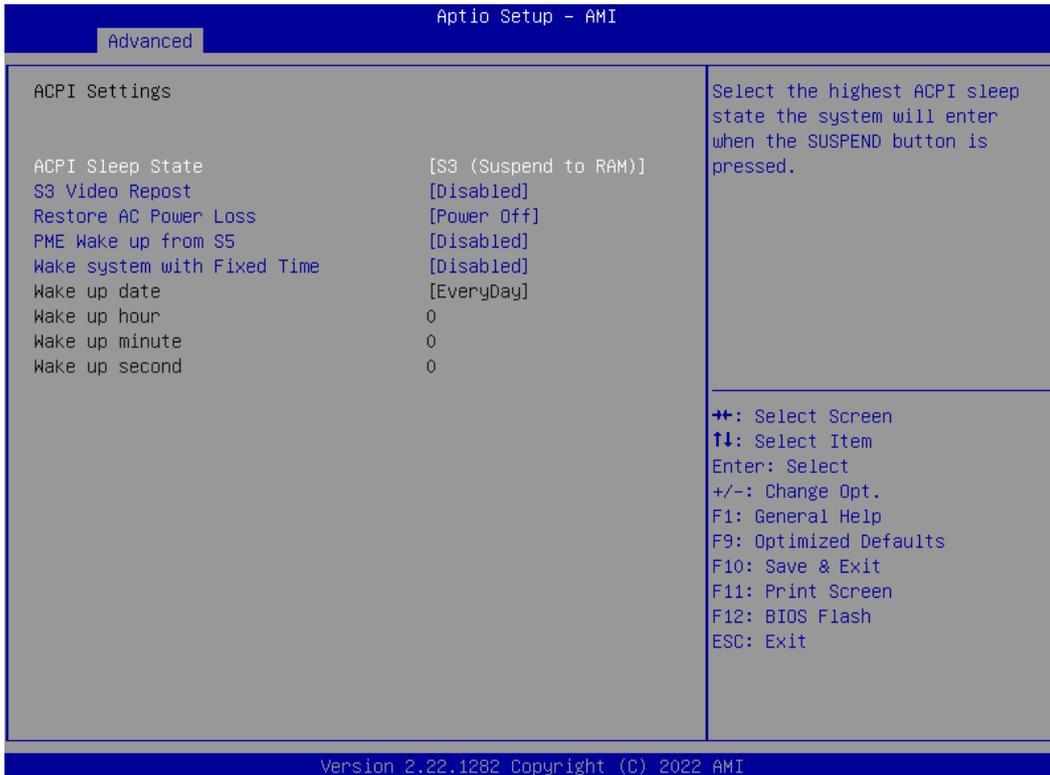
Select TPM device:

- PTT: Intel® built-in TPM. Enables PTT in SkuMgr.
- dTPM: External extended Infineon’s TPM. Disables PTT in SkuMgr.

Security Device Support

Enable or disable BIOS support for security device. OS will not show security device. TCG EFI protocol and INT1A interface will not be available.

● **ACPI Settings**



ACPI Sleep State

When the suspend button is pressed, the ACPI (Advanced Configuration and Power Interface) sleep state is S3 (Suspend to RAM).

S3 Video Repost

On enabling, Video Option ROM will be dispatched during S3 resume.

Restore AC Power Loss

Decide the state of system when power is re-applied after a power failure.

- Power Off: Keep the power off until the power button is pressed.
- Power On: Restore power to the computer.

PME Wake up from S5

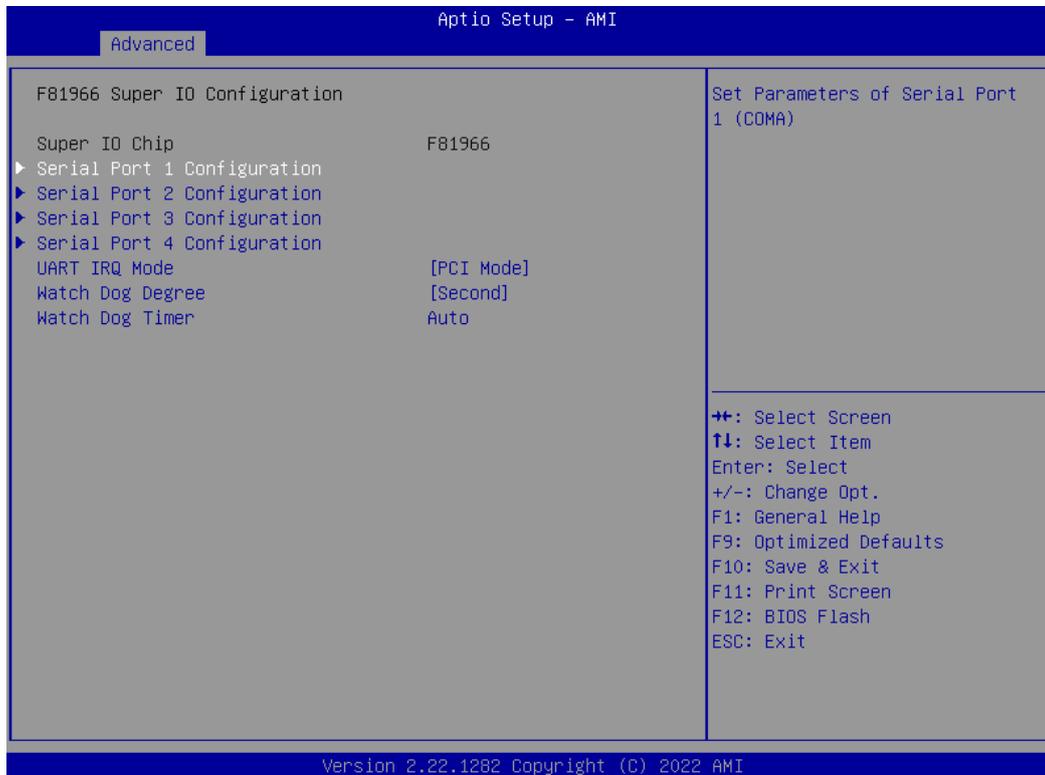
Enable system to wake from S5 using PME event.

Wake System with Fixed Time

Enable or disable system wake on alarm event. When enabled, system will wake on the hr:min:sec specified.

- **F81966 Super IO Configuration**

You can use this screen to select options for the Super IO Configuration and change the value of the selected option. A description of the selected item appears on the right side of the screen. For items marked with “▶”, please press <Enter> for more options.



Serial Port 1~4 Configuration

Use these items to set parameters related to serial port 1~4.

UART IRQ Mode

PCI IRQ sharing for OS (ex. Windows), ISA IRQ for Dos.

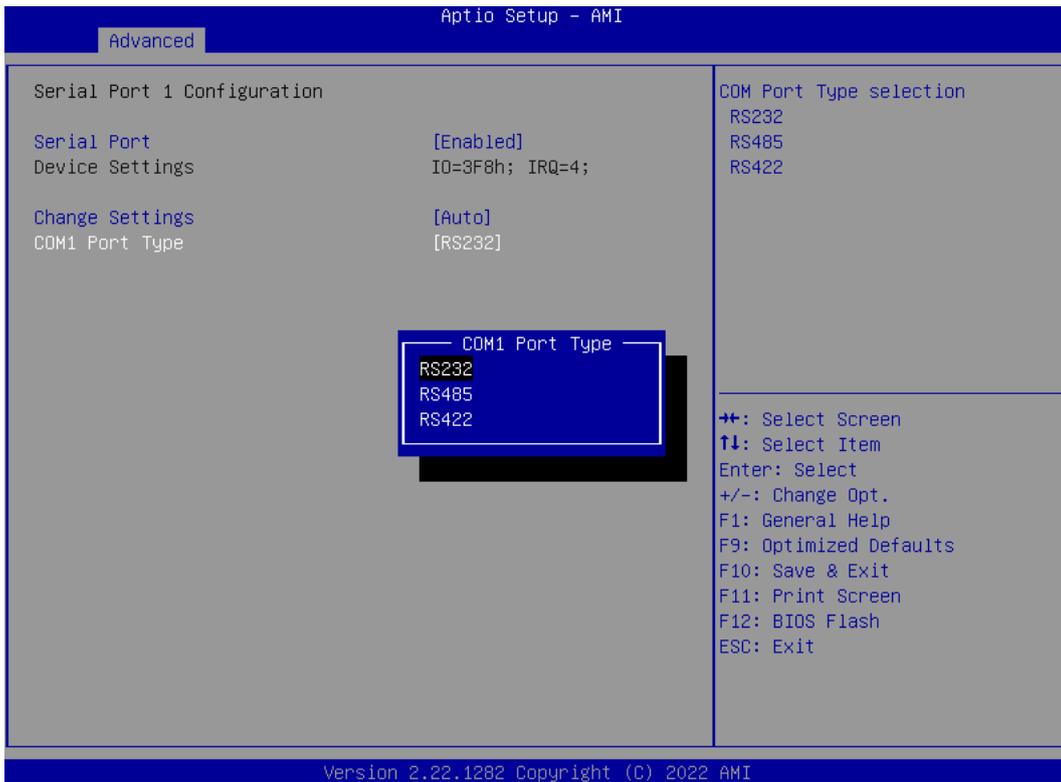
Watch Dog Degree

Watchdog degree selection in minute or second.

Watch Dog Timer

Watchdog timer value range from 1 to 255. Set 0 will disable watchdog timer.

● **Serial Port 1 Configuration**



Serial Port

Enable or disable serial port 1.

Change Settings

Select an optimal setting for Super IO device.

- Auto
- IO=3F8h, IRQ=4;
- IO=3F8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2F8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=3E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

COM1 Port Type

Select RS-232/422/485 mode for serial port 1.

● **Serial Port 2~4 Configuration**



Serial Port

Enable or disable serial port 2~4.

Change Settings

Select an optimal setting for Super IO device.

For serial port 2:

- Auto
- IO=2F8h, IRQ=3;
- IO=3F8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2F8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=3E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

For serial port 3:

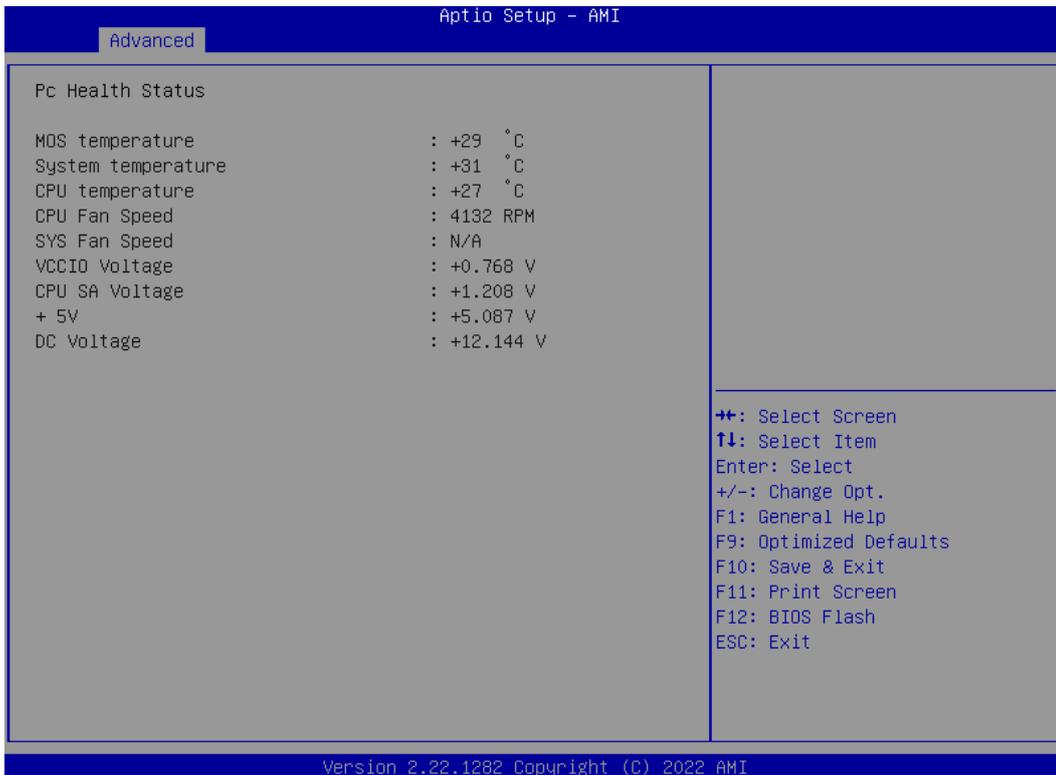
- Auto
- IO=3E8h, IRQ=7;
- IO=3E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2F0h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2E0h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

For serial port 4:

- Auto
- IO=2E8h, IRQ=7;
- IO=3E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2F0h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
- IO=2E0h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

- **Hardware Monitor**

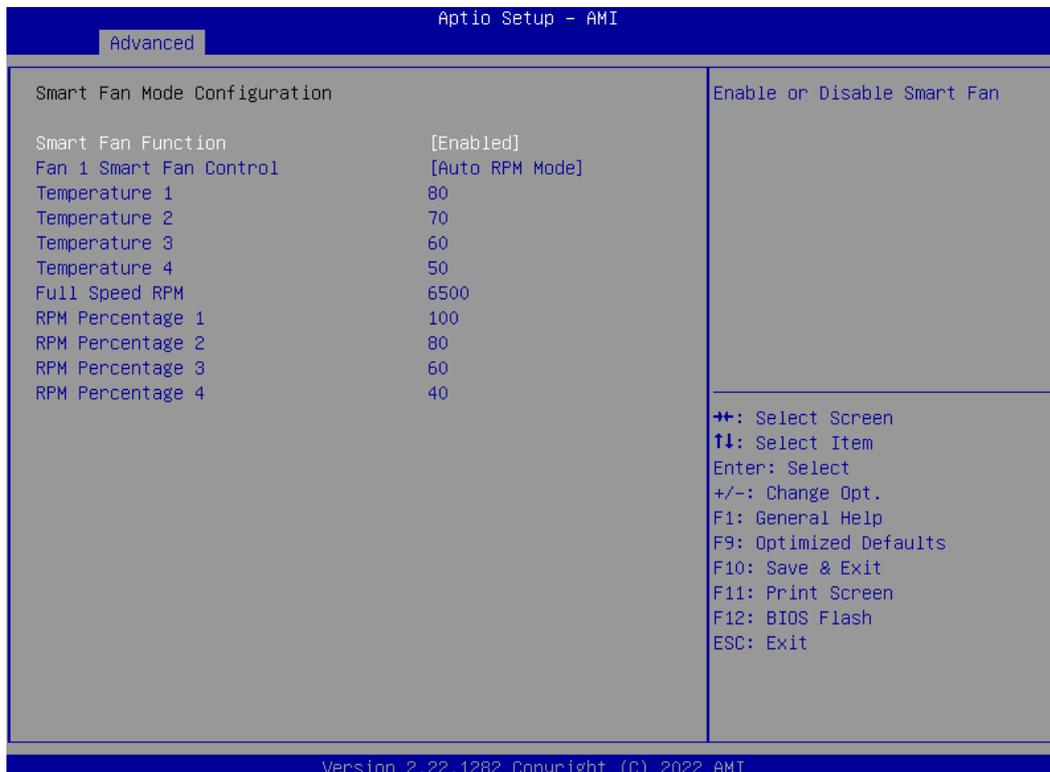
This screen monitors hardware health status.



This screen displays the temperature of system and CPU, cooling fans speed in RPM and system voltages (VCCIO, CPU SA, +5V and +12V).

- **Smart Fan Mode Configuration**

This screen allows you to configure Smart Fan mode. You can use Smart Fan function to control CN60 and CN61.



Smart Fan Function

Enable or disable Smart Fan.

Fan 1 Smart Fan Control

Select Smart Fan operating mode. Auto RPM Mode: The fan speed is controlled automatically according to temperature and RPM.

Temperature 1

Auto fan speed control. Fan speed will follow different temperature by different RPM 1~100.

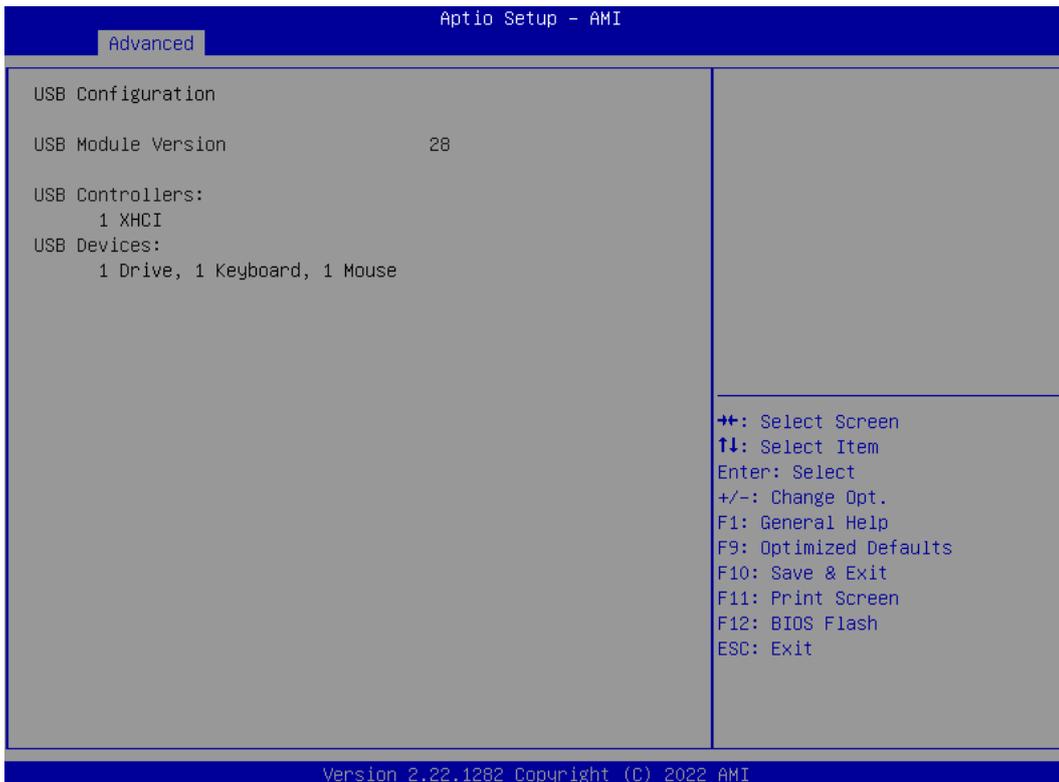
Full Speed RPM

Set fan full speed RPM.

RPM Percentage 1

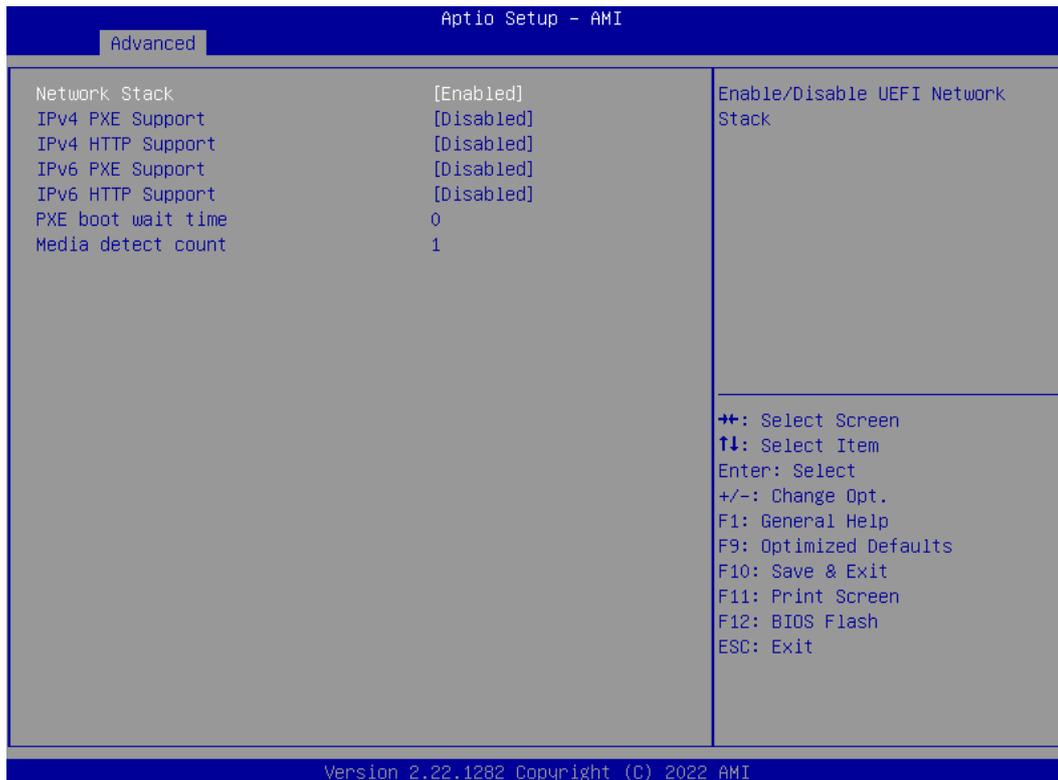
Auto fan speed control. Fan speed will follow different temperature by different RPM 1~100.

- **USB Configuration**

**USB Devices**

Display all detected USB devices.

- **Network Stack Configuration**



Network Stack

Enable or disable UEFI Network Stack.

IPv4/IPv6 PXE Support

Enable or disable IPv4 PXE boot support. If disabled, IPv4/IPv6 PXE boot support will not be available.

IPv4/IPv6 HTTP Support

Enable or disable IPv4/IPv6 HTTP boot support. If disabled, IPv4/IPv6 HTTP boot support will not be available.

PXE boot wait time

Wait time in seconds to press <ESC> key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

Number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

3.5 Chipset Menu

The Chipset menu allows users to change the advanced chipset settings. You can select any of the items in the left frame of the screen to go to the sub menus:

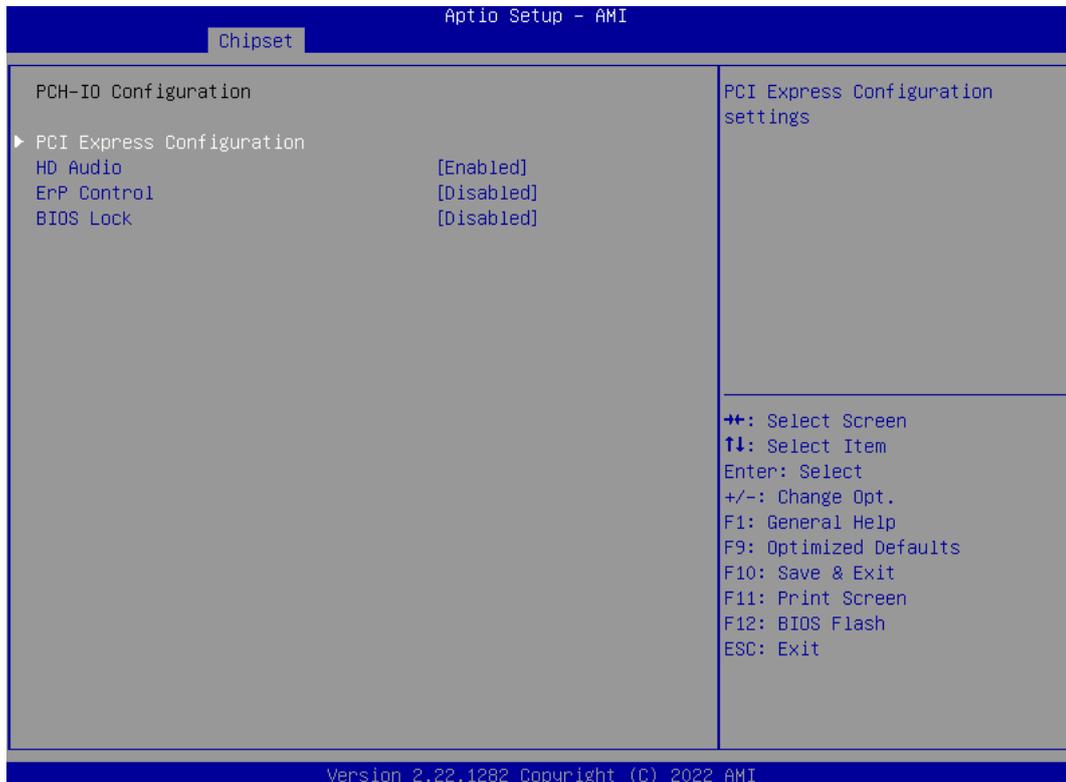
- ▶ PCH-IO Configuration
- ▶ Onboard Device
- ▶ RTD213x eDP-LVDS

For items marked with “▶”, please press <Enter> for more options.



- **PCH-IO Configuration**

This screen allows you to set PCH parameters.



HD Audio

Control detection of the HD Audio device.

- Disabled: HDA will be unconditionally disabled.
- Enabled: HDA will be unconditionally enabled.
- Auto: HDA will be enabled if present, disabled otherwise.

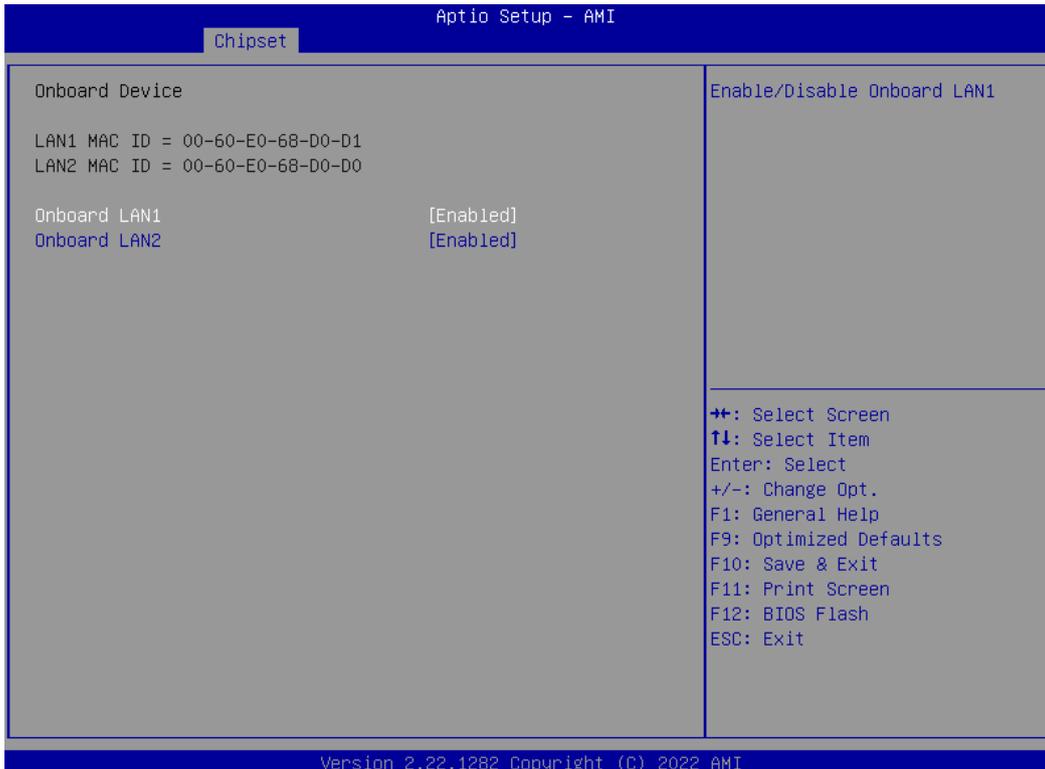
ErP Control

When ErP is enabled, system meets ErP requirement.

BIOS Lock

Enable or disable the PCH BIOS Lock Enable feature. Required to be enabled to ensure SMM protection of flash.

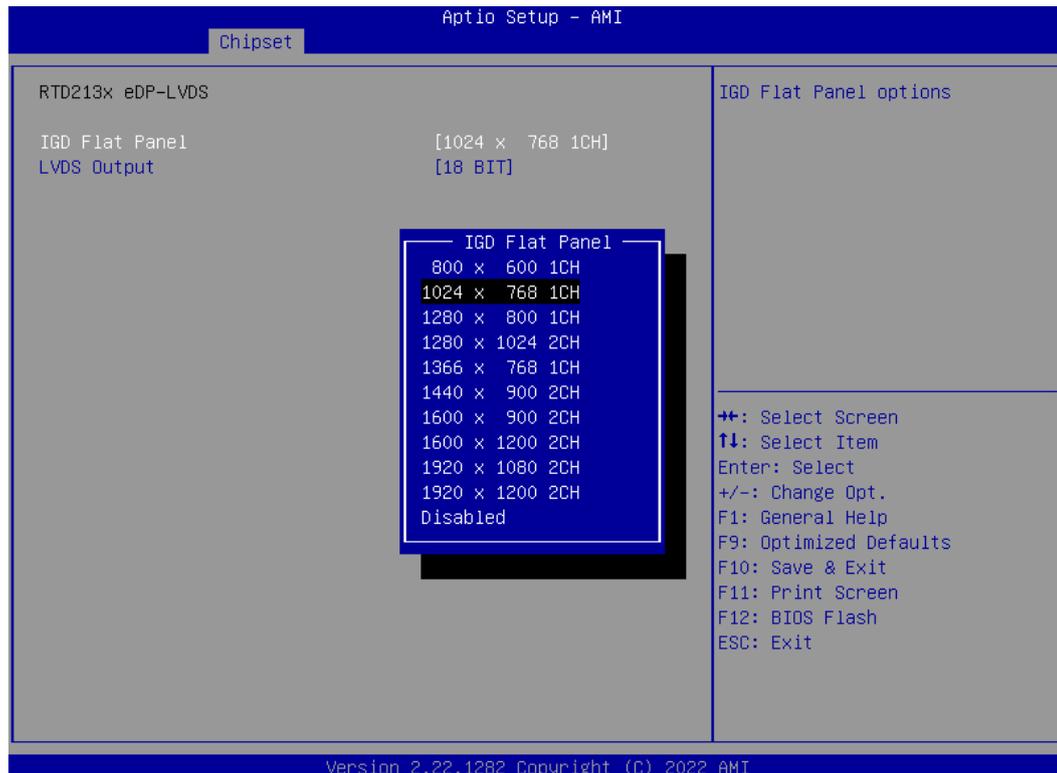
- **Onboard Device**



Onboard LAN 1/2

Enable or disable onboard LAN 1/2.

- **RTD213x eDP-LVDS**



IGD Flat Panel

Allows user to set LVDS resolution. (Default: 1024x768)



Note

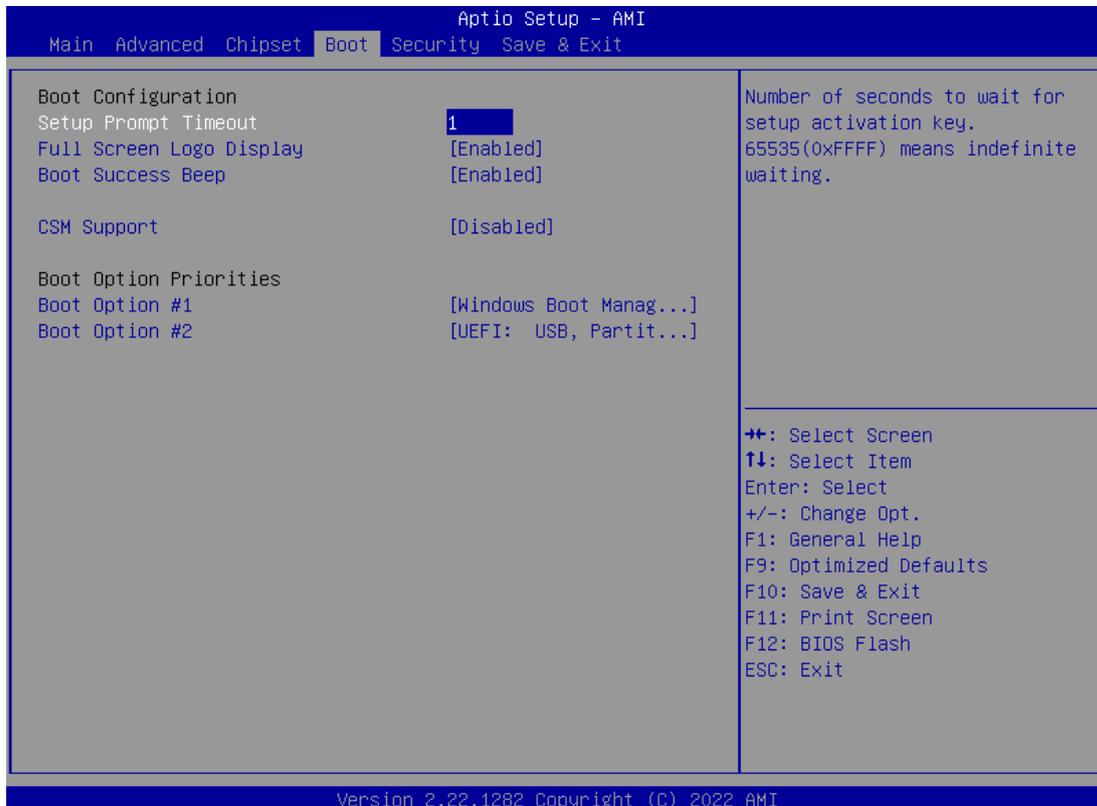
- LVDS signal divided into 1CH and 2CH.
- 1CH: 1 Channel only support resolution up to 1366x768.
- 2CH: 2 Channel support resolution higher than 1366x768.

LVDS Output

Allows user to set LVDS bit rate. (Default: 18 bit)

3.6 Boot Menu

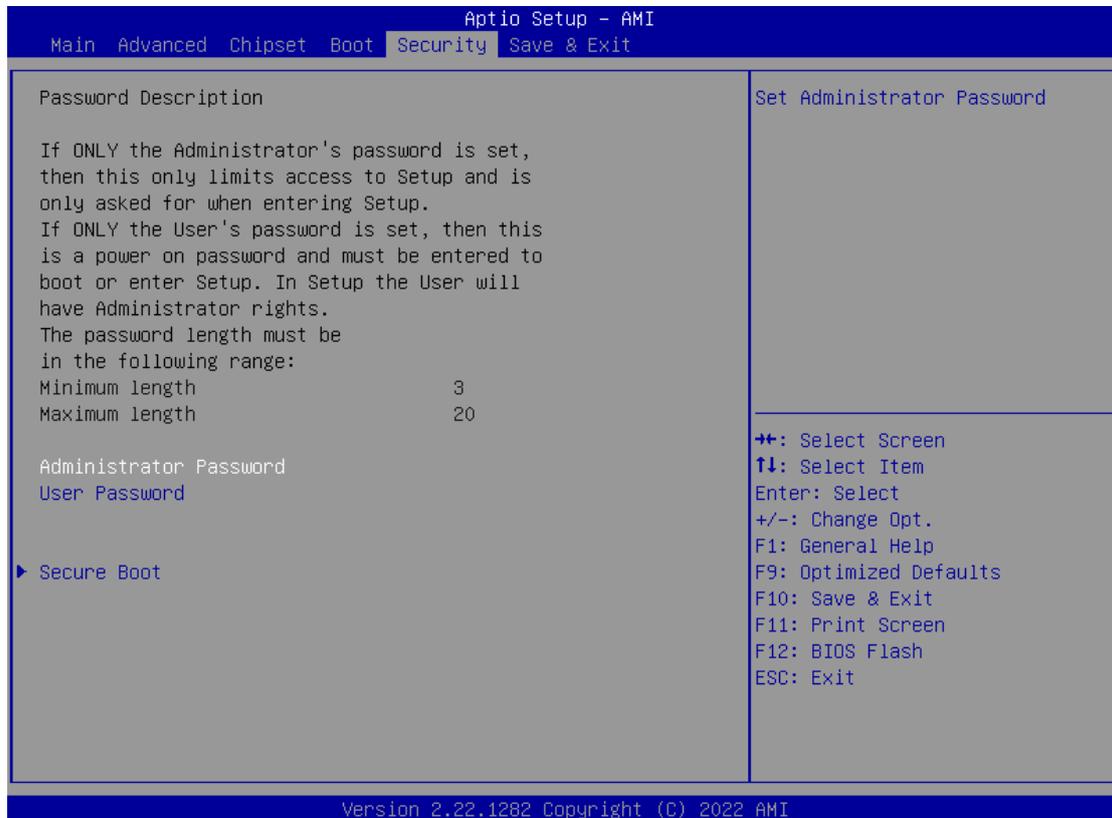
The Boot menu allows users to change boot options of the system.



- Setup Prompt Timeout**
 Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.
- Full Screen Logo Display.**
 Enable or disable full screen logo display feature.
- Boot Success Beep**
 Enable or disable beep sound after successful boot.
- CSM Support**
 Enable or disable to launch the CSM (Compatibility Support Module) support. Please do not disable unless you're running a WHCK test. If you are using Windows® 8 64-bit and all of your devices support UEFI, you may also disable CSM for faster boot speed.
- Boot Option Priorities**
 These are settings for boot priority. Specify the boot device priority sequence from the available devices.

3.7 Security Menu

The Security menu allows users to change the security settings for the system.



- **Administrator Password**
Set administrator password.
- **User Password**
Set user password.
- ▶ **Secure Boot**

- **Secure Boot**

Secure Boot is a security standard to help ensure that devices will only boot using software trusted by original equipment manufacturers (OEMs). When the computer starts, this firmware checks the signature of every boot software, including UEFI firmware drivers (also called option Rom), EFI applications, and operating systems. If the signature is valid, the computer will boot up, and this firmware allows you to control the operating system.



Secure Boot Mode

In Custom mode, Secure Boot Policy variables can be configured by a physically present User without full authentication.

Restore Factory Keys

Force system to User mode. Install factory default Secure Boot key databases.

Reset To Setup Mode

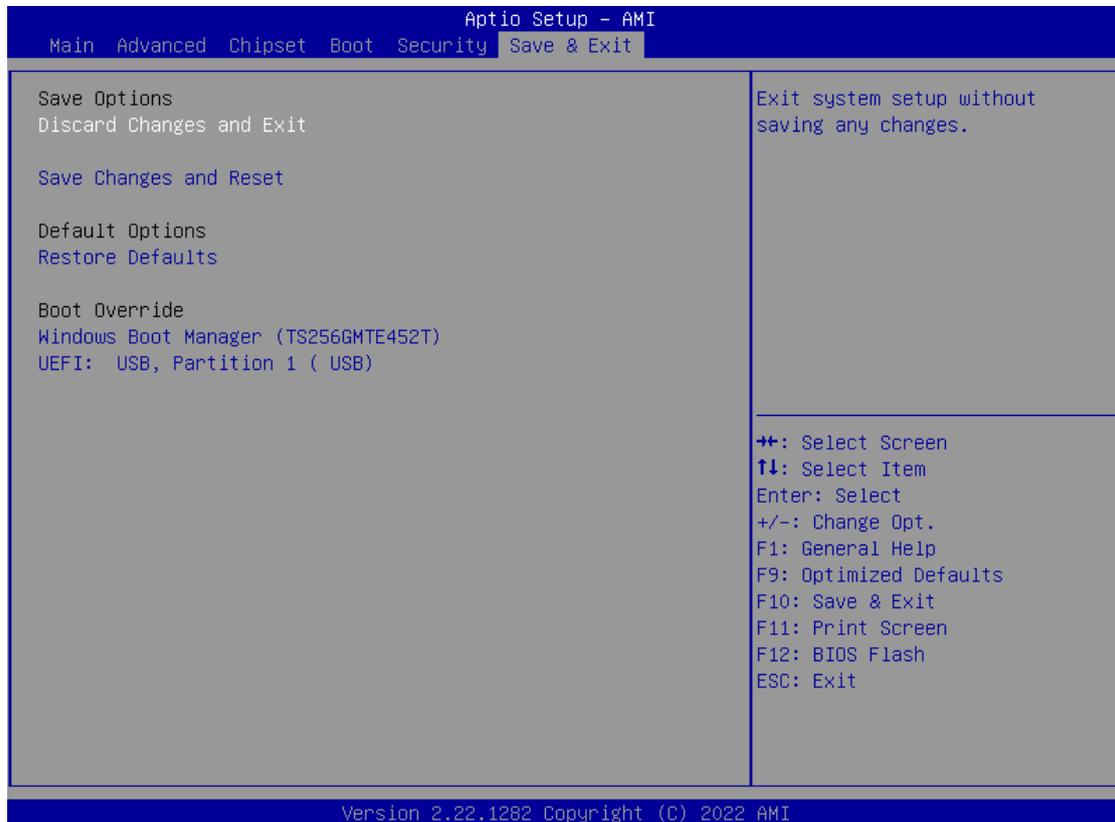
Delete all Secure Boot key databases from NVRAM.

Key Management

Enables expert users to modify Secure Boot Policy variables without full authentication.

3.8 Save & Exit Menu

The Save & Exit menu allows users to load your system configuration with optimal or fail-safe default values.



- **Discard Changes and Exit**
Exit system setup without saving any changes.
- **Save Changes and Reset**
Reset the system after saving the changes.
- **Restore Defaults**
Restore or load default values for all the setup options.
- **Boot Override**
Select a drive to immediately boot that device regardless of the current boot order.

Appendix A

Watchdog Timer

A.1 About Watchdog Timer

Software stability is major issue in most application. Some embedded systems are not watched by human for 24 hours. It is usually too slow to wait for someone to reboot when computer hangs. The systems need to be able to reset automatically when things go wrong. The watchdog timer gives us solution.

The watchdog timer is a counter that triggers a system reset when it counts down to zero from a preset value. The software starts counter with an initial value and must reset it periodically. If the counter ever reaches zero which means the software has crashed, the system will reboot.

A.2 Sample Program

```
#include "stdafx.h"
#include <windows.h>
#include <stdio.h>
#include <tchar.h>
#include <stdlib.h>

#ifdef _DEBUG
#define new DEBUG_NEW
#endif

#pragma comment (lib, "User32.lib" )

#define IDT_TIMER WM_USER + 200
#define _CRT_SECURE_NO_WARNINGS 1
#define setbit(value,x) (value |= (1<<x))
#define clrbit(value,x) (value &=~(1<<x))

HINSTANCE hinstLibDLL = NULL;
LONG WDTDATA = 0;

typedef ULONG(*LPFNDDLGETIOSPACE)(ULONG);
LPFNDDLGETIOSPACE lpFnDll_Get_IO;
typedef void(*LPFNDDLSETIOSPACE)(ULONG, ULONG);
LPFNDDLSETIOSPACE lpFnDll_Set_IO;

int _tmain(int argc, _TCHAR* argv[])
{
    int unit = 0;
    int WDTtimer = 0;
    if (hinstLibDLL == NULL)
    {
        hinstLibDLL = LoadLibrary(TEXT("diodll.dll"));
        if (hinstLibDLL == NULL)
        {
            //MessageBox("Load diodll dll error", "", MB_OK);
        }
    }
    if (hinstLibDLL)
```

```

    {
        lpFnDll_Get_IO =
(LPFNDLLGETIOSPACE)GetProcAddress(GetModuleHandle("diodll.dll"), "GetIoSpaceByte");
        lpFnDll_Set_IO =
(LPFNDLLSETIOSPACE)GetProcAddress(GetModuleHandle("diodll.dll"), "SetIoSpaceByte");

    }
    printf("Input Watch Dog Timer type, 1:Second ; 2:Minute :");
    scanf("%d",&unit);
    printf("\nInput Timer to countdown:");
    scanf("%d", &WDTtimer);
    printf("Start to countdown...");

    //==Enter MB Pnp Mode==
    lpFnDll_Set_IO(0x2e, 0x87);
    lpFnDll_Set_IO(0x2e, 0x87);
    lpFnDll_Set_IO(0x2e, 0x07);
    lpFnDll_Set_IO(0x2f, 0x07); //SET LDN 07
    //set LDN07 FA 10 to 11
    lpFnDll_Set_IO(0x2e, 0xFA);
    WDTDATA = lpFnDll_Get_IO(0x2f);
    WDTDATA = setbit(WDTDATA, 0);
    lpFnDll_Set_IO(0x2f, WDTDATA);

    if (unit == 1)
    {

        lpFnDll_Set_IO(0x2e, 0xF6);
        lpFnDll_Set_IO(0x2f, WDTtimer);

        //start watchdog counting
        lpFnDll_Set_IO(0x2e, 0xF5);
        WDTDATA = lpFnDll_Get_IO(0x2f);
        WDTDATA = setbit(WDTDATA, 5);
        lpFnDll_Set_IO(0x2f, WDTDATA);

    }
    else if (unit == 2)
    {

        //set WDT Timer
        lpFnDll_Set_IO(0x2e, 0xF6);
        lpFnDll_Set_IO(0x2f, WDTtimer);
        //set watchdog time unit to min
        lpFnDll_Set_IO(0x2e, 0xF5);
        WDTDATA = lpFnDll_Get_IO(0x2f);
        WDTDATA = setbit(WDTDATA, 3);
        lpFnDll_Set_IO(0x2f, WDTDATA);
        //start watchdog counting
        lpFnDll_Set_IO(0x2e, 0xF5);
        WDTDATA = lpFnDll_Get_IO(0x2f);
        WDTDATA = setbit(WDTDATA, 5);
        lpFnDll_Set_IO(0x2f, WDTDATA);

    }

    system("pause");

    return 0;
}

```

Appendix B

Digital I/O

B.1 About Digital I/O

The onboard digital I/O has 8 bits. Each bit can be set to function as input or output by software programming. In default, all pins are pulled high with +5V level (according to main power). The BIOS default settings are 4 inputs and 4 outputs.

B.2 Sample Program

```
#include "stdafx.h"

#ifdef _DEBUG
#define new DEBUG_NEW
#endif

#include <windows.h>
#include <stdio.h>
#include <tchar.h>
#include <stdlib.h>

#pragma comment (lib, "User32.lib" )

#define IDT_TIMER WM_USER + 200
#define _CRT_SECURE_NO_WARNINGS 1
#define setbit(value,x) (value |= (1<<x))
#define clrbit(value,x) (value &=~(1<<x))
#define GPIO_HIGH 1
#define GPIO_LOW 0

HINSTANCE hinstLibDLL = NULL;

LONG u8AHData = 0;
LONG u88HData = 0;
LONG u89HData = 0;

static int DI0status = 1;
static int DI1status = 1;
static int DI2status = 1;
static int DI3status = 1;

typedef ULONG(*LPFNDDLGETIOSPACE)(ULONG);
LPFNDDLGETIOSPACE lpFnDll_Get_IO;
typedef void(*LPFNDDLSETIOSPACE)(ULONG, ULONG);
LPFNDDLSETIOSPACE lpFnDll_Set_IO;

int _tmain(int argc, _TCHAR* argv[])
{
    if (hinstLibDLL == NULL)
    {
        hinstLibDLL = LoadLibrary(TEXT("dioidll.dll"));
        if (hinstLibDLL == NULL)
        {

```

```

        //MessageBox("Load diodll.dll error", "", MB_OK);
    }
}
if (hinstLibDLL)
{
    lpFnDll_Get_IO =
(LPFNDLLGETIOSPACE)GetProcAddress(GetModuleHandle("diodll.dll"), "GetIoSpaceByte");
    lpFnDll_Set_IO =
(LPFNDLLSETIOSPACE)GetProcAddress(GetModuleHandle("diodll.dll"), "SetIoSpaceByte");
}
/*
printf("Input Watch Dog Timer type, 1:Second ; 2:Minute :");
scanf("%d",&unit);
printf("\nInput Timer to countdown:");
scanf("%d", &WDTimer);
printf("Start to countdown...");
*/
//==Enter MB Pnp Mode==
lpFnDll_Set_IO(0x2e, 0x87);
lpFnDll_Set_IO(0x2e, 0x87);
//LDN 06
lpFnDll_Set_IO(0x2e, 0x07);
lpFnDll_Set_IO(0x2f, 0x06);
//set LDN06 88h =OF
//88h <0> = 1 GPIO80 DO0 output mode set 1 or input mode set 0
lpFnDll_Set_IO(0x2e, 0x88);
u88HData = lpFnDll_Get_IO(0x2f);
u88HData = setbit(u88HData, 0);
lpFnDll_Set_IO(0x2f, u88HData);
// 88h <1> =1 GPIO81 DO1 output mode set 1 or input mode set 0
lpFnDll_Set_IO(0x2e, 0x88);
u88HData = lpFnDll_Get_IO(0x2f);
u88HData = setbit(u88HData, 1);
lpFnDll_Set_IO(0x2f, u88HData);
// 88h <2> =1 GPIO82 DO2 output mode set 1 or input mode set 0
lpFnDll_Set_IO(0x2e, 0x88);
u88HData = lpFnDll_Get_IO(0x2f);
u88HData = setbit(u88HData, 2);
lpFnDll_Set_IO(0x2f, u88HData);
// 88h <3> =1 GPIO83 DO3 output mode set 1 or input mode set 0
lpFnDll_Set_IO(0x2e, 0x88);
u88HData = lpFnDll_Get_IO(0x2f);
u88HData = setbit(u88HData, 3);
lpFnDll_Set_IO(0x2f, u88HData);

//set 89 FF-F0
// 89 <0> = 0 set GPIO 80 outputs 0 when in output mode
lpFnDll_Set_IO(0x2e, 0x89);
u89HData = lpFnDll_Get_IO(0x2f);
u89HData = clrbit(u89HData, 0);
lpFnDll_Set_IO(0x2f, u89HData);

// 89 <1> = 0
lpFnDll_Set_IO(0x2e, 0x89);
u89HData = lpFnDll_Get_IO(0x2f);
u89HData = clrbit(u89HData, 1);
lpFnDll_Set_IO(0x2f, u89HData);

//89 <2> = 0
lpFnDll_Set_IO(0x2e, 0x89);
u89HData = lpFnDll_Get_IO(0x2f);
u89HData = clrbit(u89HData, 2);
lpFnDll_Set_IO(0x2f, u89HData);

//89 <3> = 0

```

```

lpFnDll_Set_IO(0x2e, 0x89);
u89HData = lpFnDll_Get_IO(0x2f);
u89HData = clrbits(u89HData, 3);
lpFnDll_Set_IO(0x2f, u89HData);

while (1)
{
    //Get GPIO 8x Status
    lpFnDll_Set_IO(0x2e, 0x8A);
    u8AHDData = lpFnDll_Get_IO(0x2f);
    lpFnDll_Set_IO(0x2f, u8AHDData);
    if (0x10 & u8AHDData) //GPIO84 DI0 status
    {
        DI0status = GPIO_HIGH;
    }
    else
    {
        DI0status = GPIO_LOW;
    }
    if (0x20 & u8AHDData) //GPIO85 DI1 status
    {
        DI1status = GPIO_HIGH;
    }
    else
    {
        DI1status = GPIO_LOW;
    }
    if (0x40 & u8AHDData) //GPIO86 DI2 status
    {
        DI2status = GPIO_HIGH;
    }
    else
    {
        DI2status = GPIO_LOW;
    }
    if (0x80 & u8AHDData) //GPIO87 DI3 status
    {
        DI3status = GPIO_HIGH;
    }
    else
    {
        DI3status = GPIO_LOW;
    }
    if ((DI0status == GPIO_LOW && DI1status == GPIO_LOW) && (DI2status ==
GPIO_LOW && DI3status == GPIO_LOW))
    {
        printf("All DINPUT status Low\n");
    }
    else if((DI0status == GPIO_HIGH && DI1status == GPIO_HIGH) && (DI2status ==
GPIO_HIGH && DI3status == GPIO_HIGH))
    {
        printf("All DINPUT status High\n");
    }
    Sleep(1000);
}
system("pause");
return 0;
}

```

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Appendix C

BIOS Update

With the BIOS-Flasher utility you can easily update motherboard BIOS without having to enter operating system. In this appendix you may learn how to do it in just a few steps. Please read and follow the instructions below carefully.

C.1 How to update system BIOS using <F12> key

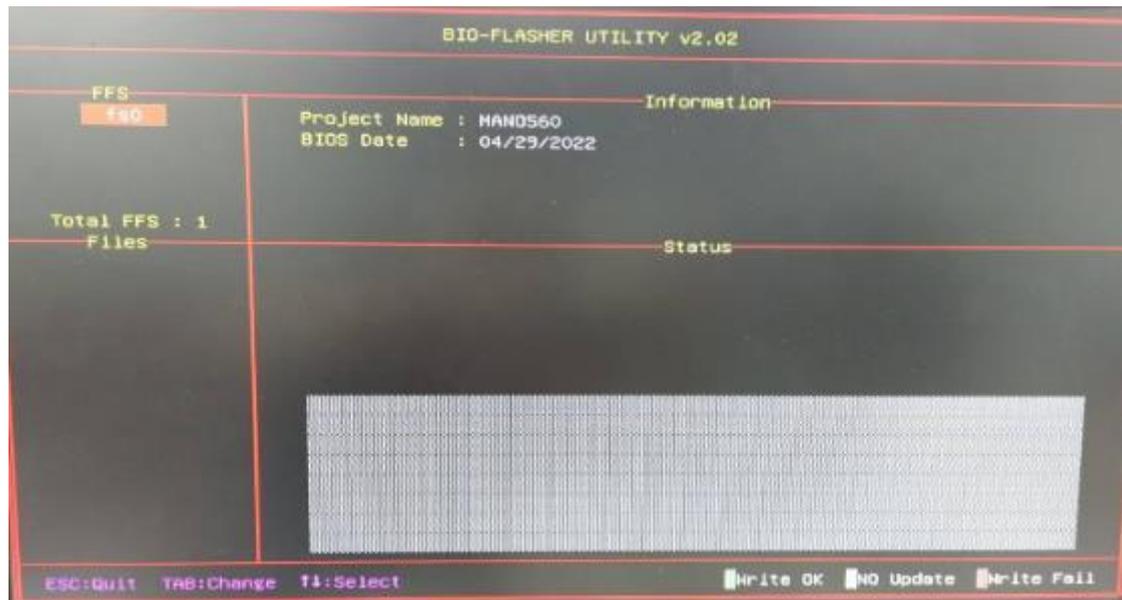
1. Copy the BIOS file to USB flash drive. Only FAT32 file system format can be recognized by BIOS-Flasher utility. Right click the USB drive folder icon and choose "Properties" from the drop down menu. In the resulting dialog box, you could see the file system. Please make sure the format is FAT32.

名稱	修改日期	類型	大小
MA560429.BA	2022/4/29 下午 02:08	BA 檔案	32,768 KB

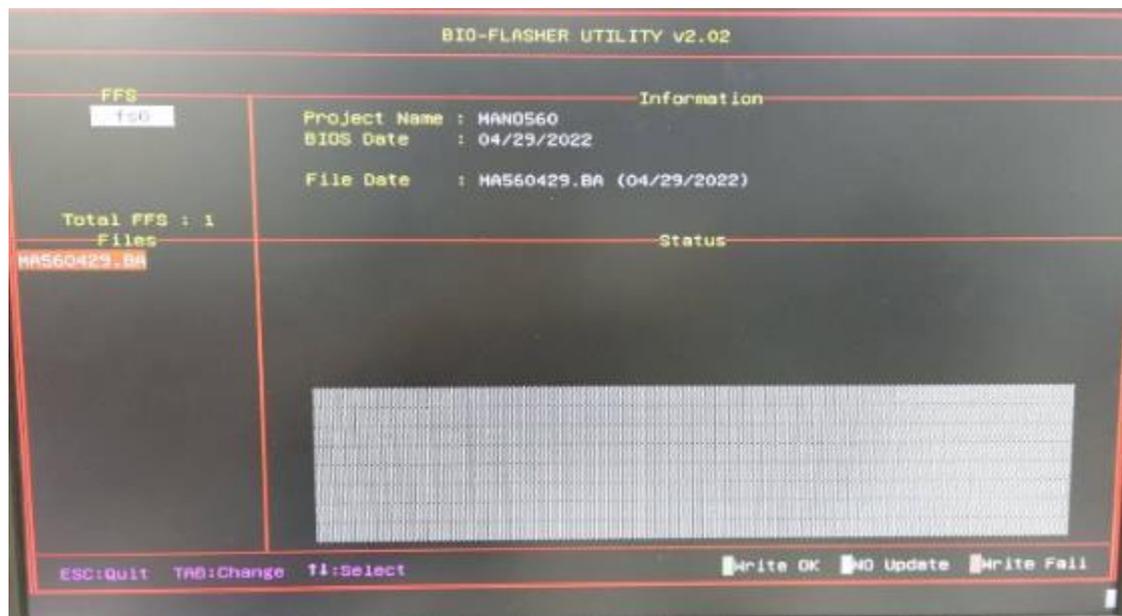


2. Insert your USB flash drive into USB port on the system you want to update and boot it.

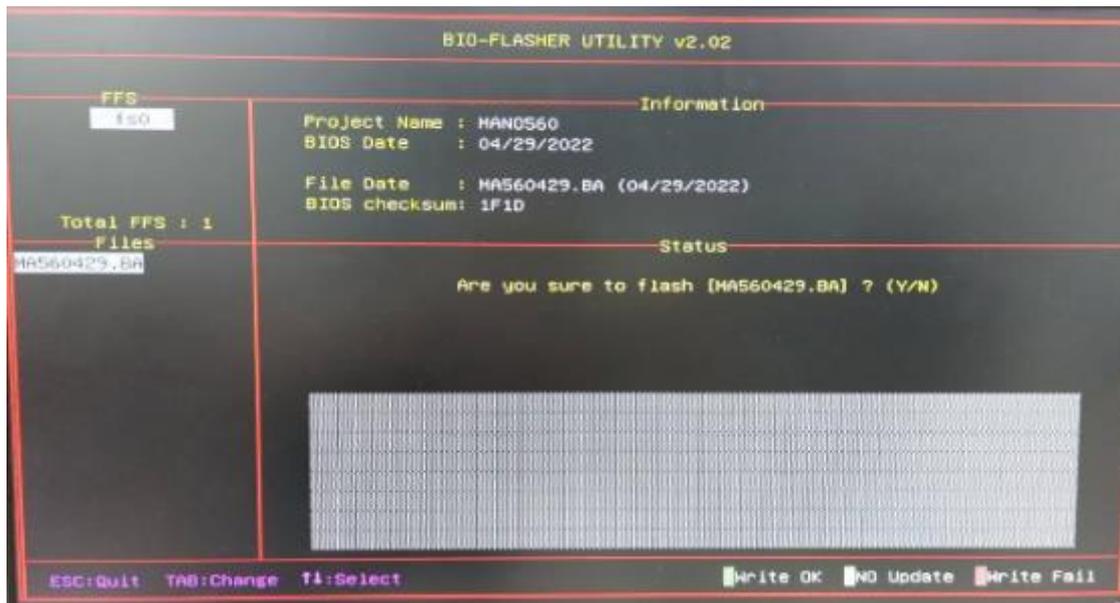
3. After booting up, press <F12> to enter the BIOS update screen.



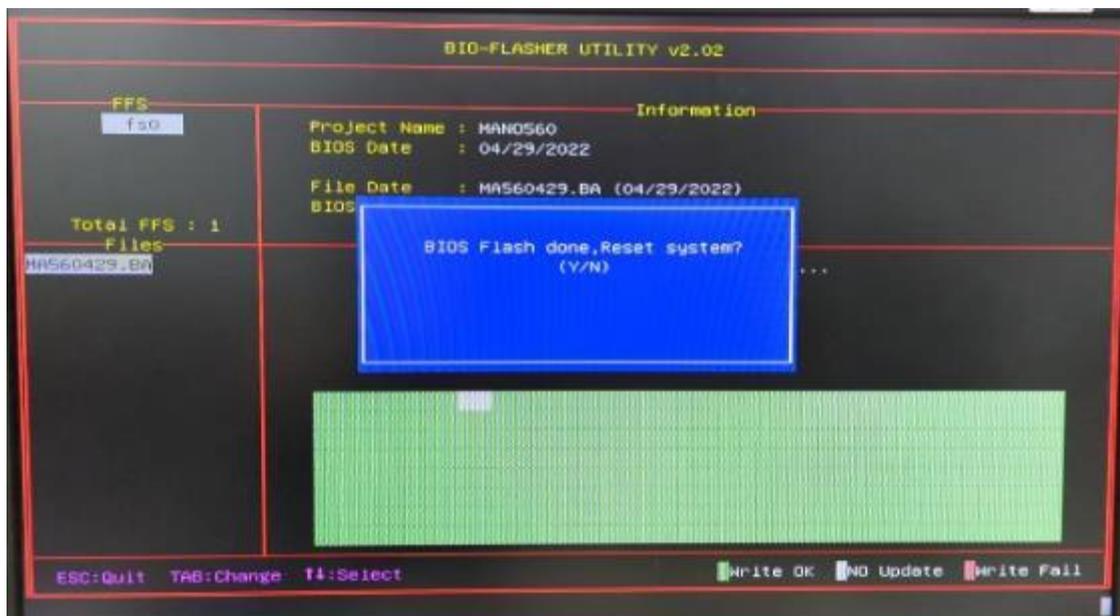
4. Then press <F12> again to enter next screen. Now you can see ini figure below, the "fs0" is the detected USB device. If multiple USB flash drives or hard drives are connected, there will be several optional devices such as "fs1", "fs2" and so on. Please make sure to choose the correct USB drive and press <Enter> to open it.



- Choose the new BIOS file, then press “Y”.



- The update will take a few minutes, do not turn off the power or interrupt the update process. Please wait until the utility completes the entire BIOS update process.
- The following screen will appear once the update is completed. Please press “Y” to restart.



- After the system restarts, please press to enter BIOS setup screen. Press <F9> Load Optimized Default and then press <F10> to save and exit.