USER'S MANUAL

PICO570

Intel® Core™ Ultra Processors (Series 1), Pico-ITX Board

User's Manual

AXIOMTEK

www.axiomtek.com

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CAUTION

If you replace wrong batteries, it causes the danger of explosion. It is recommended by the manufacturer that you follow the manufacturer's instructions to only replace the same or equivalent type of battery, and dispose of used ones.

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Printed in Taiwan

ESD Precautions

Computer boards have integrated circuits sensitive to static electricity. To prevent chipsets from electrostatic discharge damage, please take care of the following jobs with precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before holding the board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. It discharges static electricity from your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

Trademarks Acknowledgments

Table of Contents

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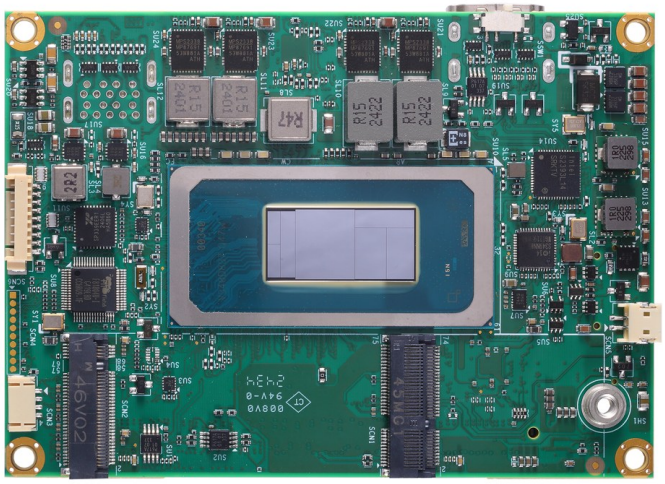
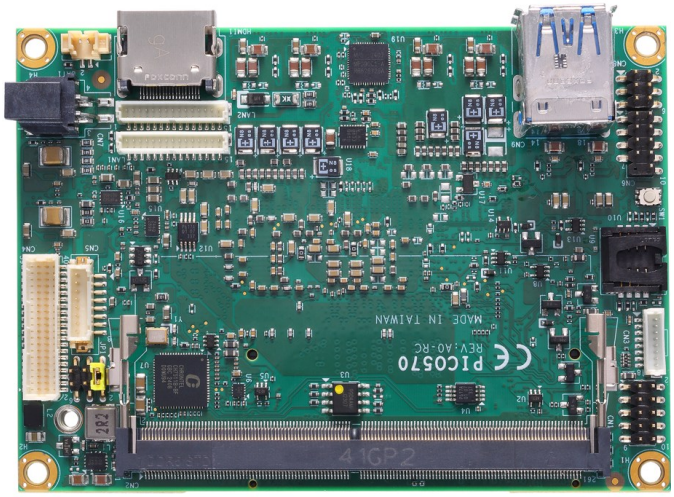
Section 1
Introduction





The PICO570 is a Pico-ITX board with the Intel® Core™ Ultra Processors (Series 1) that delivers outstanding system performance through high-bandwidth interfaces, multiple I/O functions for interactive applications and various embedded computing solutions.

The PICO570 has one 262-pin SO-DIMM socket for DDR5 5600MHz SO-DIMM memory with maximum capacity up to 64GB. It also features one Gigabit Ethernet, one 2.5 Gigabit Ethernet, two USB 3.2 Gen 2 and two USB 2.0 high speed compliant and one M.2 Key E for wireless module. Additionally, it provides you with unique embedded features such as one serial port which support RS-232/422/485 and 2.5” form factor that applies an extensive array of PC peripherals. The board can be enhanced by its built-in watchdog timer function, a special industrial feature not commonly seen on other motherboards.

1.1 Features

- PICO570 - Intel® Core™ Ultra Processors (Series 1)
- One DDR5 SO-DIMM supports up to 64GB memory capacity
- Two USB 3.2 Gen 2 ports and Two USB 2.0 ports
- One Gigabit Ethernet ports and one 2.5 Gigabit Ethernet
- LVDS/HDMI
- M.2 Key E 2230
- M.2 Key M 2280

1.2 Specifications

- **CPU**
  - Intel® Core™ Ultra Processors (Series 1)
    - Intel® Core™ Ultra 7 Processor 155U
    - Intel® Core™ Ultra 5 Processor 125U

- **Thermal Solution**
  - Passive

- **Operating Temperature**
  - -20°C~+60°C

- **BIOS**
  - American Megatrends Inc. UEFI (Unified Extensible Firmware Interface) BIOS
  - 256Mbit SPI Flash, DMI, Plug and Play
  - PXE Ethernet Boot ROM

- **System Memory**
  - One 262-pin unbuffered DDR5 SO-DIMM socket
  - Maximum up to 64GB DDR5 5600MHz memory

- **Serial Port**
  - Controller: Fintek F81804 (maximum baud rate: 921 kbps)
  - One serial port supports RS-232/422/485

- **Storage**
  - One M.2 Key M connector (22mm x 80mm)
  - PCIe 4.0 x4 or SATA interface

- **USB Interface**
  - Two USB 3.2 Gen 2 ports (10Gbps) in type A on the rear I/O
  - Two USB 2.0 ports in 2x5-pin internal wafer connector

  Display
  - A standard HDMI connector: Support HDMI 2.1. The HDMI resolution is up to 3840x2160 @120Hz
  - One 2x20-pin connector for 18/24-bit single and dual channel LVDS (with one 8-pin wafer connector for inverter control). LVDS resolution is up to 1920x1200 in 24-bit dual channel.

- **Watchdog Timer**
  - 1~255 seconds or minutes; up to 255 levels

- **Ethernet**
  - Two Ethernet ports
    LAN1: Intel® I226-V supports 2500/1000/100/10Mbps Gigabit/Fast Ethernet with Wake-on-LAN and PXE Boot ROM in 1x15-pin internal wafer connector
    LAN2: Intel® I219-LM supports 1000/100/10Mbps Gigabit/Fast Ethernet with Wake-on-LAN and PXE Boot ROM in 1x15-pin internal wafer connector

- **Audio**
  - HD audio link without codec in 1x8-pin internal wafer connector

- **Expansion Interface**
  - One M.2 Key E connector (22mm x 30mm)
  - PCIe 4.0 x1 and USB 2.0 interfaces

- **Power Input**
  - One 2x2-pin connector
  - +12V DC-in only at minimum 12V/2A
  - Auto power on function supported

- **Power Management**
  - ACPI (Advanced Configuration and Power Interface)

- **Form Factor**
  - Pico-ITX form factor

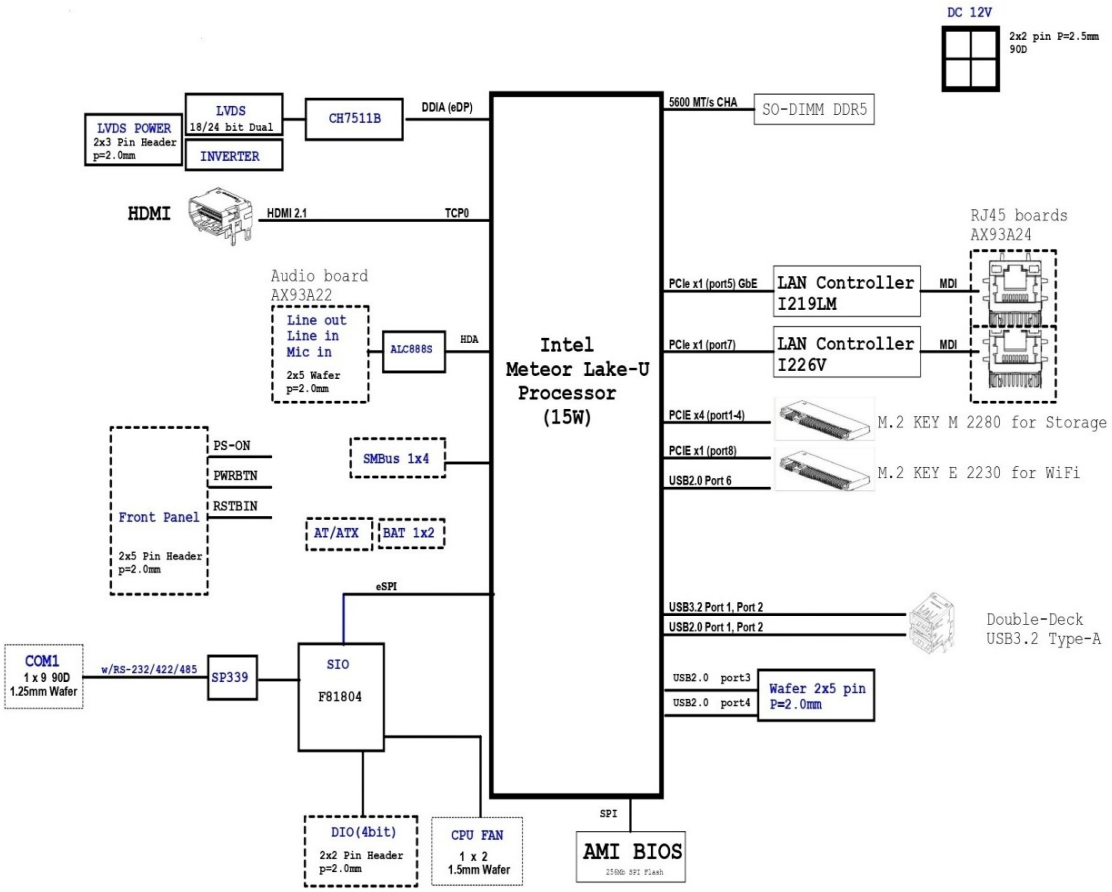
Note

All specifications and images are subject to change without notice.

1.3 Utilities

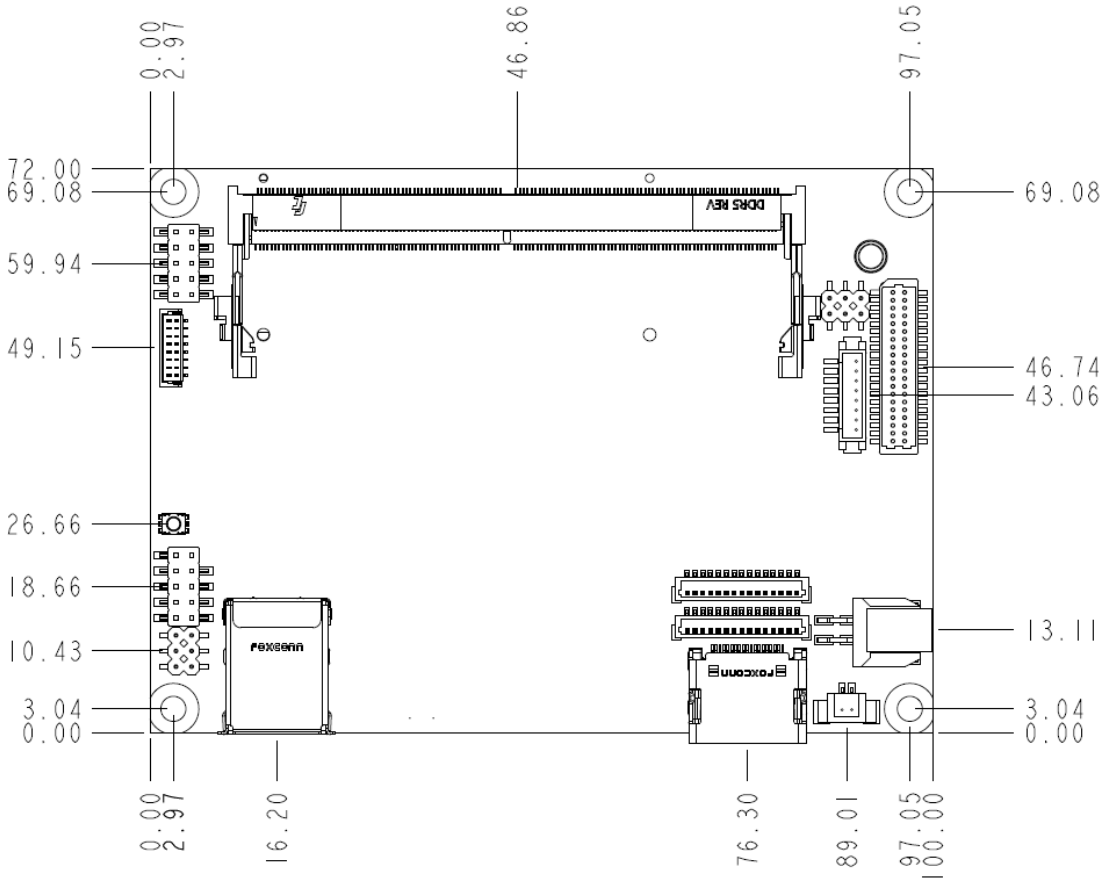
- Chipset and graphics driver
- Ethernet driver
- ME driver
- Axiomtek eAPI3.0 SDK and Driver

1.4 Block Diagram

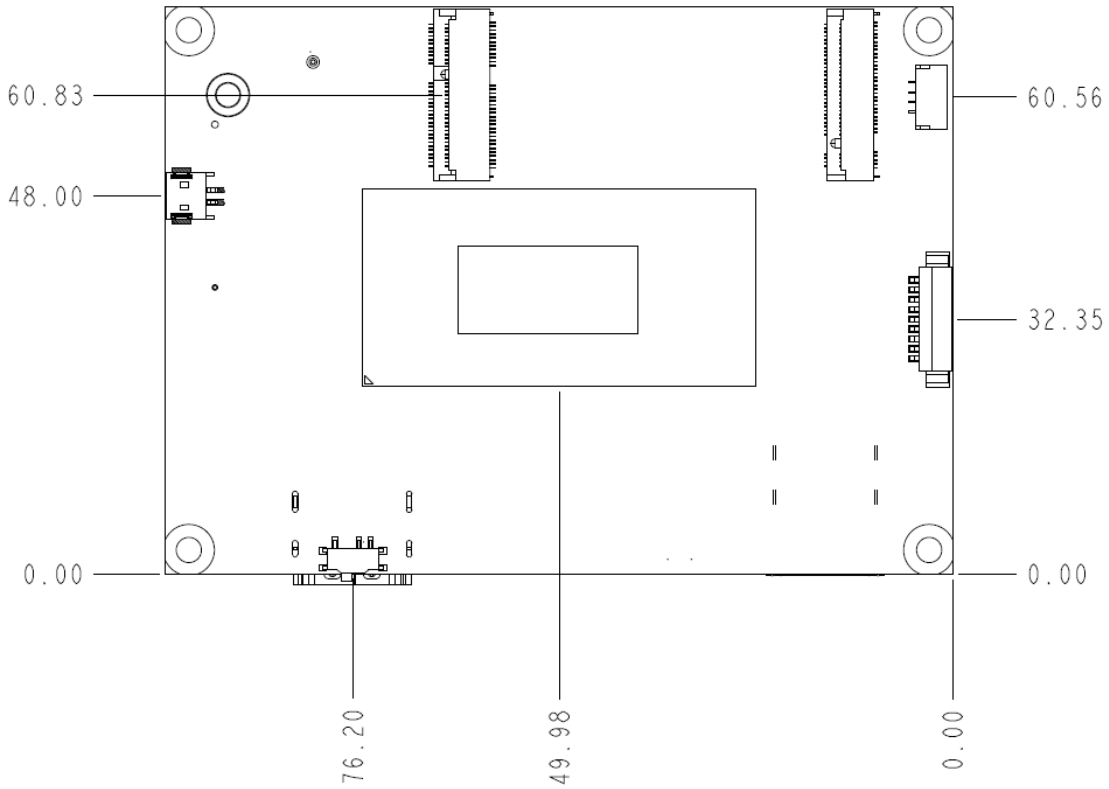


Section 2
Board and Pin Assignments

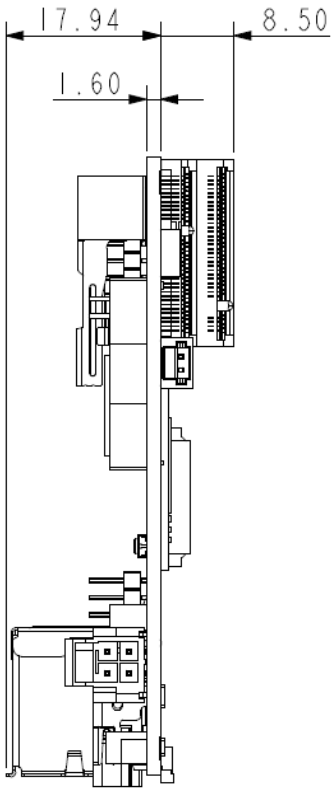
2.1 Board Dimensions and Fixing Holes



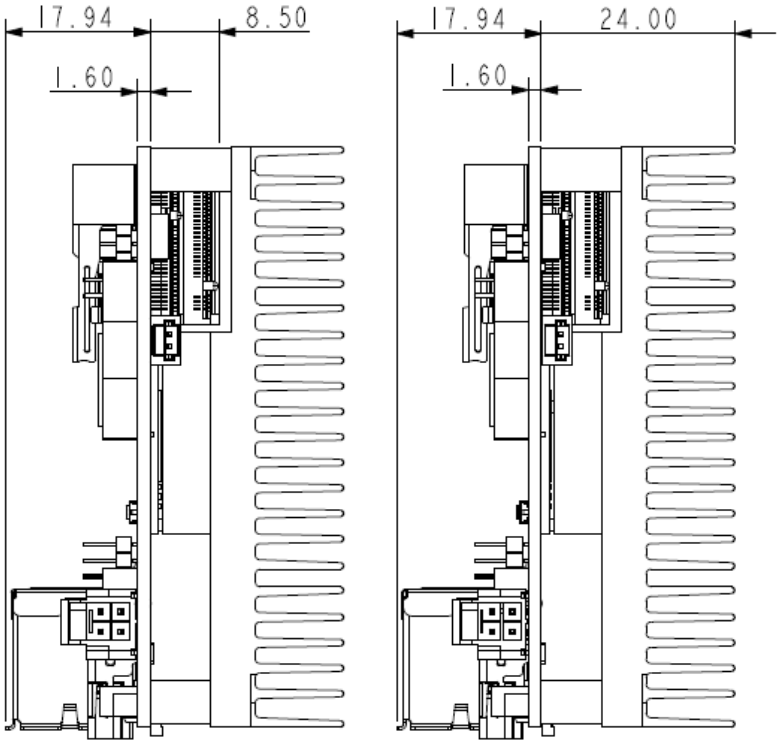
Top View



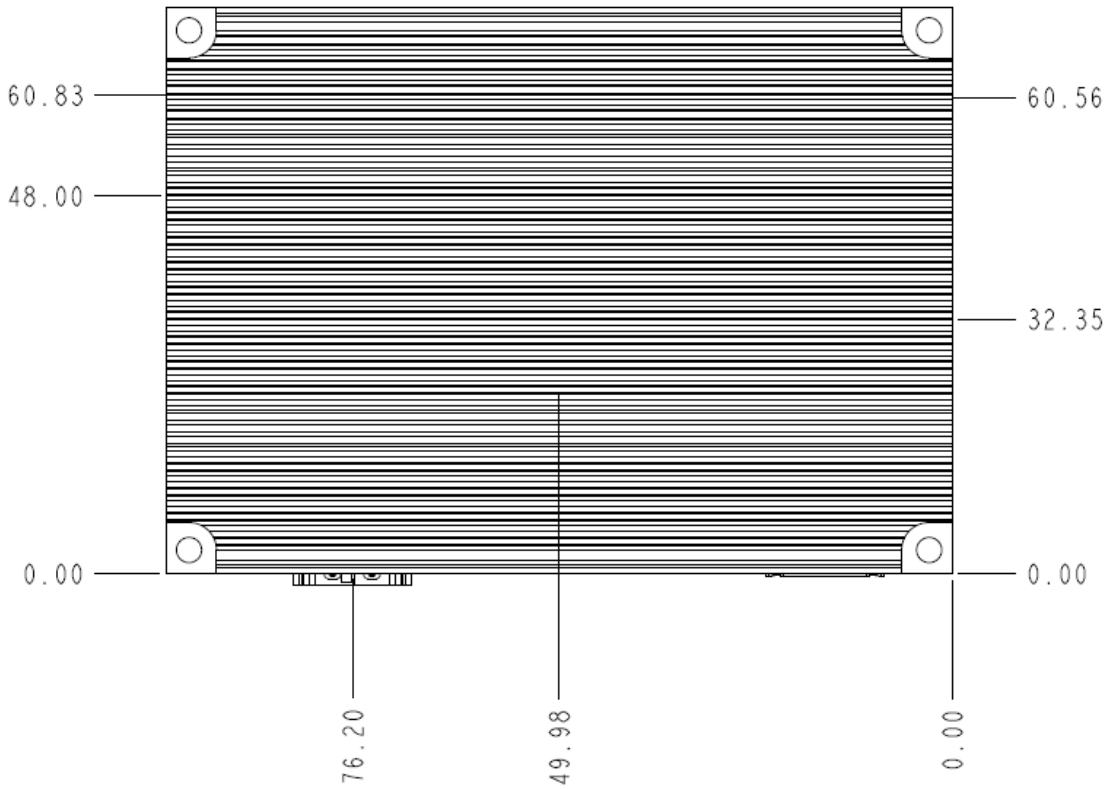
Bottom View



Side View

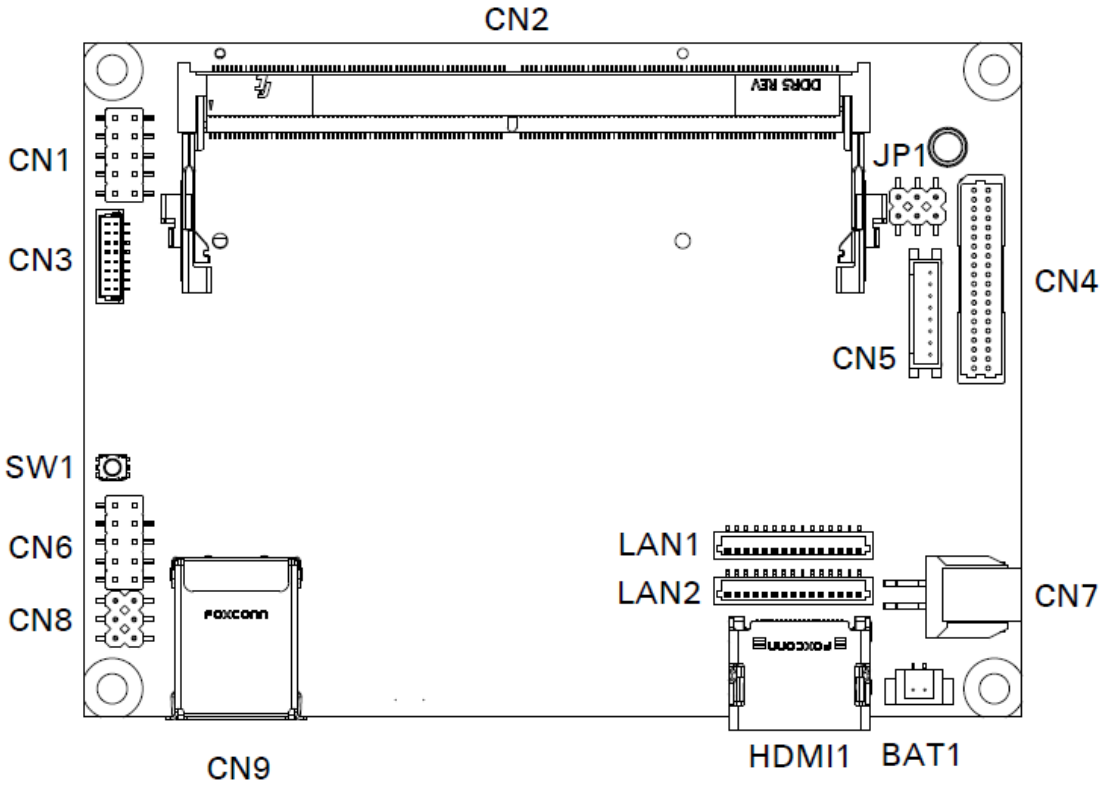


Side View (Board + Heatsink)

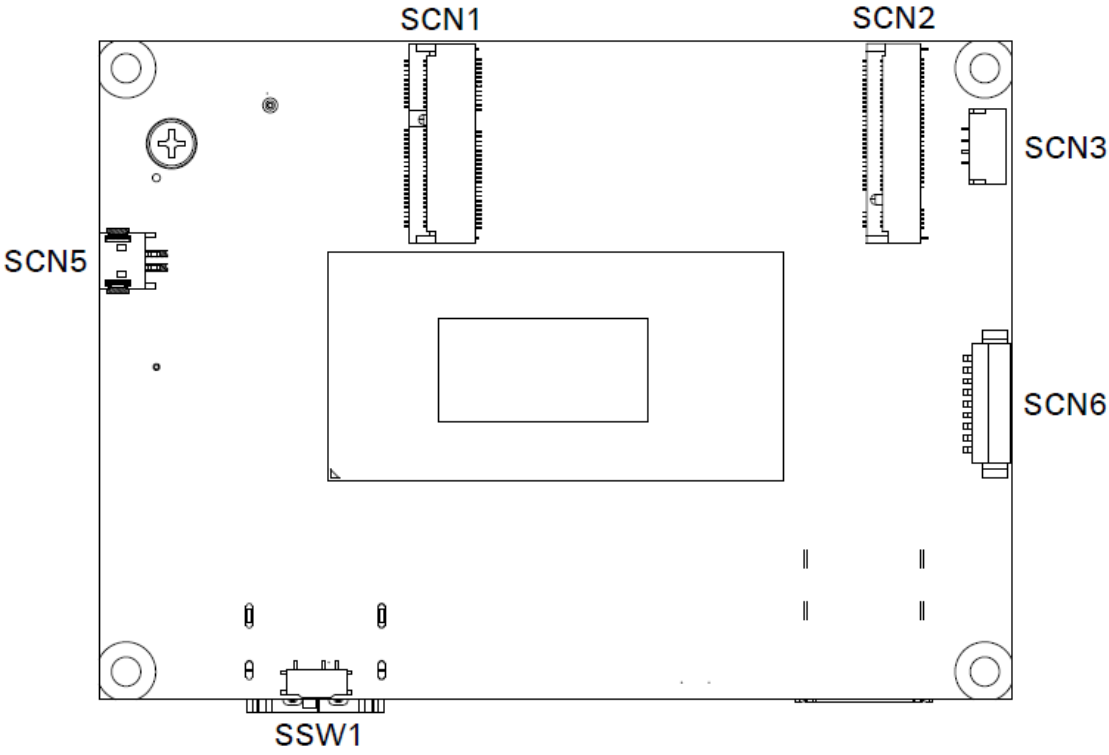


Top view (Board + Cooler)

2.2 Board Layout



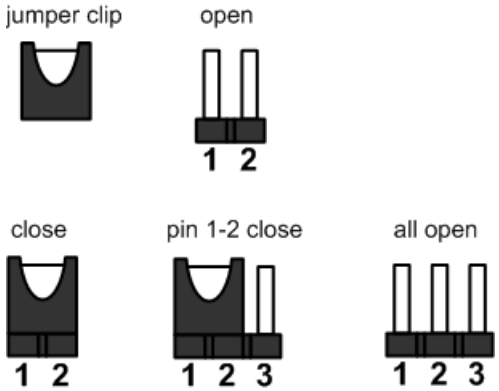
Top View



Bottom View

2.3 Jumper and Switch Settings

Jumper is a small component consisting of jumper clip and jumper pins. Install jumper clip on 2 jumper pins to close. And remove jumper clip from 2 jumper pins to open. Below illustration shows how to set up jumper.



Properly configure jumper and switch settings on the PICO570 to meet your application purpose. Below you can find a summary table of jumper, switch and onboard default settings.

Note

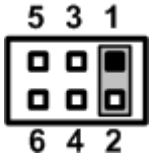
Once the default jumper or switch setting needs to be changed, please do it under power-off condition.

Jumper and Switch	Description	Setting
JP1	LVDS +3.3V/+5V/+12V Voltage Selection Default: +3.3V Level	1-2 Close
SW1	Restore BIOS Optimal Defaults Default: Normal Operation	Release
SSW1	Auto Power On Default: Disable	1-2 Close

2.3.1 LVDS +3.3V/+5V/+12V Voltage Selection (JP1)

The board supports voltage selection for flat panel displays. Use this jumper to set LVDS connector (CN4, see section 2.4.3) pin 1~6 VCCM to +3.3V, +5V or +12V. To prevent hardware damage, before connecting please make sure that the input voltage of flat panel is correct.

Function	Setting
+3.3V level (Default)	1-2 close
+5V level	2-4 close
+12V level	5-6 close



2.3.2 Restore BIOS Optimal Defaults (SW1)

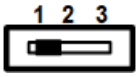
Use SW1 to clear CMOS. Press the tact switch for at least 3 seconds to restore BIOS optimal defaults.

Function	Setting
Normal (Default)	Release
Restore BIOS optimal defaults	Press

2.3.3 Auto Power On (SSW1)

If SSW1 is enabled for power input, the system will be automatically power on without pressing soft power button. If SSW1 is disabled for power input, it is necessary to manually press soft power button to power on the system.

Function	Setting
Disable auto power on (Default)	1-2 close
Enable auto power on	2-3 close



2.4 Connectors

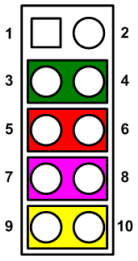
Signals go to other parts of the system through connectors. Loose or improper connection might cause problems, please make sure all connectors are properly and firmly connected. Here is a summary table of connectors on the hardware.

Connector	Description
CN1	Front Panel Wafer Connector
CN2	DDR5 SO-DIMM Socket
CN3	HD Audio Connector
CN4	LVDS Connector
CN5	Inverter Connector
CN6	USB 2.0 Wafer Connector
CN7	Power Connector
CN8	Digital I/O Wafer Connector
CN9	USB 3.2 Gen 2 Type A Port
LAN1	I226-V Ethernet Connector
LAN2	I219-LM Ethernet Connector
HDMI1	HDMI 2.1 Connector
SCN1	M.2 Key E Connector
SCN2	M.2 Key M Connector
SCN3	SMBus Connector
SCN5	Fan Connector
SCN6	COM Connector
BAT1	CMOS Battery Connector

2.4.1 Front Panel Connector (CN1)

This is a 2x5-pin header (pitch=2.0mm) for front panel interface.

Pin	Signal	Pin	Signal
1	GND	2	PS_ON_N
3	GND	4	+5V
5	GND	6	PSIN_N
7	GND	8	RST_N
9	N/A	10	+5V



Power Status
Pin 1 and pin 2 are for power status button; letting user know the power status of this board.

Power LED
Pin 4 connects anode (+) of LED and pin 3 connects cathode (-) of LED. The power LED lights up when the system is powered on

Power On/Off Button
Pin 5 and 6 connect the power button on front panel to CPU board, which allows users to turn on or off power supply.

System Reset Switch
Pin 7 and 8 connect the case-mounted reset switch that reboots your computer without turning off the power switch. It is a better way to reboot your system for a longer life of system power supply.

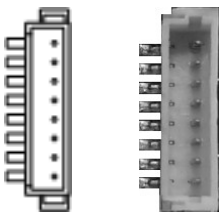
2.4.2 HD Audio Connector (CN3)

This is an 8-pin (pitch=1.0mm) wafer connector, which is compliant with JST BM08B-SRSS-TB, for HD audio interface.

Note

It is recommended to connect AX93A22 to have Mic in/Line in and Line out.

Pin	Signal
1	+5V_SBY
2	HDA_BCLK
3	HDA_SDI0
4	HDA_SDO
5	HDA_SYNC
6	HDA_RST_N
7	SLP_S3#
8	GND

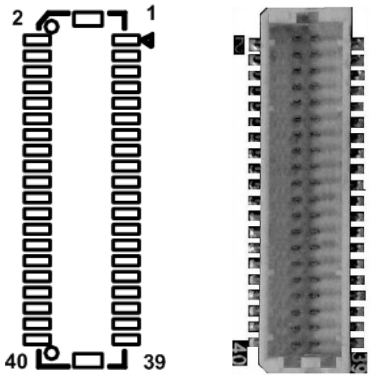


2.4.3 LVDS Connector (CN4)

This is a 2x20-pin (pitch=1.0mm) connector, which is compliant with JST SM40B-SRDS-G-TF, for LVDS LCD interface. You are strongly recommended to connect it with matching connector, SHDR-40VS-B. Pins 1~6 VCCM can be set to +3.3V, +5V or +12V by configuring JP1 (see section 2.3.1).

18-bit single channel

Pin	Signal	Pin	Signal
1	VCCM	2	VCCM
3	VCCM	4	VCCM
5	VCCM	6	VCCM
7	N.C	8	N.C
9	GND	10	GND
11	N.C	12	N.C
13	N.C	14	N.C
15	GND	16	GND
17	N.C	18	N.C
19	N.C	20	N.C
21	GND	22	GND
23	Channel A D0-	24	N.C
25	Channel A D0+	26	N.C
27	GND	28	GND
29	Channel A D1-	30	N.C
31	Channel A D1+	32	N.C
33	GND	34	GND
35	Channel A D2-	36	Channel A CLK-
37	Channel A D2+	38	Channel A CLK+
39	GND	40	GND



24-bit single channel

Pin	Signal	Pin	Signal
1	VCCM	2	VCCM
3	VCCM	4	VCCM
5	VCCM	6	VCCM
7	N.C	8	N.C
9	GND	10	GND
11	N.C	12	N.C
13	N.C	14	N.C
15	GND	16	GND
17	N.C	18	N.C
19	N.C	20	N.C
21	GND	22	GND
23	Channel A D0-	24	N.C
25	Channel A D0+	26	N.C
27	GND	28	GND
29	Channel A D1-	30	Channel A D3-
31	Channel A D1+	32	Channel A D3+
33	GND	34	GND
35	Channel A D2-	36	Channel A CLK-
37	Channel A D2+	38	Channel A CLK+
39	GND	40	GND

18-bit dual channel

Pin	Signal	Pin	Signal
1	VCCM	2	VCCM
3	VCCM	4	VCCM
5	VCCM	6	VCCM
7	N.C	8	N.C
9	GND	10	GND
11	N.C	12	Channel B D0-
13	N.C	14	Channel B D0+
15	GND	16	GND
17	Channel B CLK-	18	Channel B D1-
19	Channel B CLK+	20	Channel B D1+
21	GND	22	GND
23	Channel A D0-	24	Channel B D2-
25	Channel A D0+	26	Channel B D2+
27	GND	28	GND
29	Channel A D1-	30	N.C
31	Channel A D1+	32	N.C
33	GND	34	GND
35	Channel A D2-	36	Channel A CLK-
37	Channel A D2+	38	Channel A CLK+
39	GND	40	GND

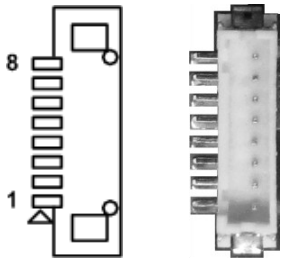
24-bit dual channel

Pin	Signal	Pin	Signal
1	VCCM	2	VCCM
3	VCCM	4	VCCM
5	VCCM	6	VCCM
7	N.C	8	N.C
9	GND	10	GND
11	Channel B D3-	12	Channel B D0-
13	Channel B D3+	14	Channel B D0+
15	GND	16	GND
17	Channel B CLK-	18	Channel B D1-
19	Channel B CLK+	20	Channel B D1+
21	GND	22	GND
23	Channel A D0-	24	Channel B D2-
25	Channel A D0+	26	Channel B D2+
27	GND	28	GND
29	Channel A D1-	30	Channel A D3-
31	Channel A D1+	32	Channel A D3+
33	GND	34	GND
35	Channel A D2-	36	Channel A CLK-
37	Channel A D2+	38	Channel A CLK+
39	GND	40	GND

2.4.4 Inverter Connector (CN5)

This is an 8-pin (pitch=1.25mm) connector, which is compliant with Hirose DF13-8P-1.25V, for inverter. You are strongly recommended to use the matching connector, DF13-8S-1.25C, to avoid malfunction.

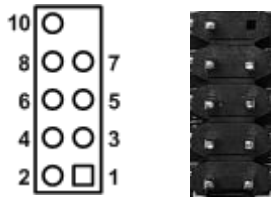
Pin	Signal
1	+12V (+12V level)
2	+12V (+12V level)
3	+5V
4	LVDS Enable Control
5	GND
6	GND
7	GND
8	LVDS Brightness Control



2.4.5 USB 2.0 Wafer Connector (CN6)

This is a 2x5-pin cut pin 9 (pitch=2.0mm) wafer connector, which is compliant with Hirose DF11-10DP-2DSA, for installing versatile USB 2.0 compliant interface peripherals.

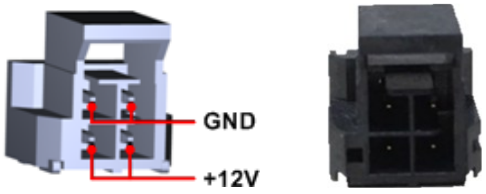
Pin	Signal	Pin	Signal
1	+5V_SBY	2	+5V_SBY
3	USB #3_D-	4	USB #4_D-
5	USB #3_D+	6	USB #4_D+
7	GND	8	GND
		10	GND



2.4.6 Power Connector (CN7)

This is a 2x2pin (pitch=2.5mm) connector, which is compliant with Molex 1054051104.

Pin	Signal
1	GND
2	GND
3	+12V
4	+12V

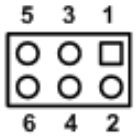


2.4.7 Digital I/O Wafer Connector (CN8)

The connector is a 2x3-pin unshrouded header (2.0mm pitch), compatible with Samtec TMM-103-01-L-D-SM. For cable assembly, please use a 2.0mm pitch non-polarized female housing or a standard 2.0mm IDC socket.

The board is equipped with a 4-bit digital I/O that meets requirements for a system customary automation control. The digital I/O can be configured to control cash drawers and sense warning signals from an Uninterrupted Power System (UPS), or perform store security control. You may use software programming to control these digital signals, please refer to Appendix B.

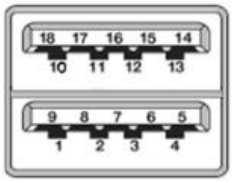
Pin	Signal	Pin	Signal
1	DIO 0	2	DIO 3
3	DIO 1	4	DIO 2
5	+5V	6	GND

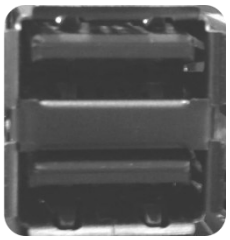


2.4.8 USB 3.2 Gen 2 Type A Port (CN9)

The board provides two USB Type-A connectors compliant with USB 3.2 Gen 2 (10 Gbps) for connecting peripherals such as keyboard, mouse, and scanner.

Pin	Signal	Pin	Signal
1	+5V	10	+5V
2	USB_Data0-	11	USB_Data1-
3	USB_Data0+	12	USB_Data1+
4	GND	13	GND
5	SSRX0-	14	SSRX1-
6	SSRX0+	15	SSRX1+
7	GND	16	GND
8	SSTX0-	17	SSTX1-
9	SSTX0+	18	SSTX1+





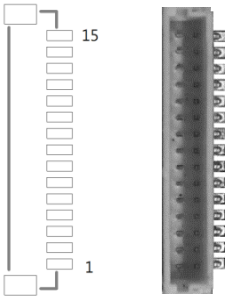
2.4.9 I226-V Ethernet Connector (LAN1)

This is a 15-pin (pitch=1.0mm) connector which is compliant with JST BM15B-SRSS-TB for Ethernet port interface, supporting 2500/1000/100/10Mbps speeds.

Note

It is recommended to connect the AX93A24 to provide an RJ45 connector for network cable installation.

Pin	Signal
1	GND
2	LED_ACT
3	+3.3VA
4	GND
5	DP0
6	DN0
7	DP1
8	DP2
9	DN2
10	DN1
11	DP3
12	DN3
13	GND
14	LED_2500
15	LED_1000



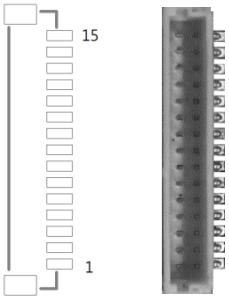
2.4.10 I219-LM Ethernet Connector (LAN2)

This is a 15-pin (pitch=1.0mm) connector which is compliant with JST BM15B-SRSS-TB for Ethernet port interface, supporting 1000/100/10Mbps speeds

Note

It is recommended to connect the AX93A24 to provide an RJ45 connector for network cable installation.

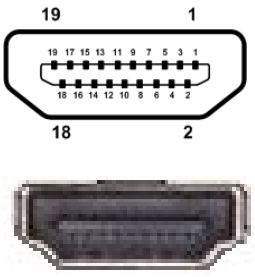
Pin	Signal
1	GND
2	LED_ACT
3	+3.3VA
4	GND
5	DP0
6	DN0
7	DP1
8	DP2
9	DN2
10	DN1
11	DP3
12	DN3
13	GND
14	LED_100
15	LED_1000



2.4.11 HDMI 2.1 Connector (HDMI1)

HDMI 2.1 supports up to 4K resolution at 120Hz, bandwidth and 16-bit color depth. It enables advanced features such as Dynamic HDR, eARC, and Variable Refresh Rate (VRR), while maintaining full backward compatibility with HDMI 2.0.

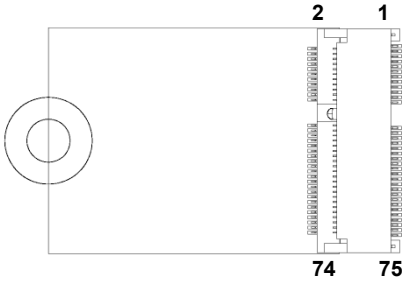
Pin	Signal	Pin	Signal
1	HDMI OUT_DATA2+	2	GND
3	HDMI OUT_DATA2-	4	HDMI OUT_DATA1+
5	GND	6	HDMI OUT_DATA1-
7	HDMI OUT_DATA0+	8	GND
9	HDMI OUT_DATA0-	10	HDMI OUT_Clock+
11	GND	12	HDMI OUT_Clock-
13	HDMI_CEC	14	N.C
15	HDMI OUT_SCL	16	HDMI OUT_SDA
17	GND	18	+5V
19	HDMI_HTPLG		



2.4.12 M.2 Key E Connector (SCN1)

The SCN1 is a M.2 2230 Key E connector supporting PCIe 4.0 x1 and USB2.0. It is recommended to install the M.2 wireless module with 22mm width and 30mm length.

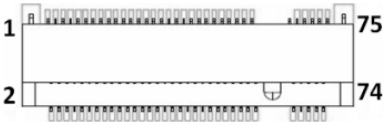
Pin	Signal	Pin	Signal
1	GND	2	+3.3V_SBY
3	USB2_DP10	4	+3.3V_SBY
5	USB2_DN10	6	NC
7	GND	8	NC
9	NC	10	NC
11	NC	12	NC
13	GND	14	NC
15	NC	16	NC
17	NC	18	GND
19	GND	20	UART_BT_WAKE
21	NC	22	NC
23	NC	24	Key E
25	Key E	26	
27		28	
29		30	
31		32	NC
33	GND	34	NC
35	PCIE8_TXP	36	NC
37	PCIE8_TXN	38	CLINK_RST
39	GND	40	CLINK_DAT
41	PCIE8_RXP	42	CLINK_CLK
43	PCIE8_RXN	44	NC
45	GND	46	NC
47	CLKOUT5_KEY_E_DP	48	NC
49	CLKOUT5_KEY_E_DN	50	SUSCLK (+3.3V Level Reserve)
51	GND	52	PLTRST_2_3P3_N
53	CLKREQ1_KEY_E	54	W_DIS2# (+3.3V Level)
55	WAKE_N	56	W_DI12# (+3.3V Level)
57	GND	58	NC
59	NC	60	NC
61	NC	62	NC
63	GND	64	NC
65	NC	66	NC
67	NC	68	NC
69	GND	70	NC
71	NC	72	+3.3V_SBY
73	NC	74	+3.3V_SBY
75	GND		



2.4.13 M.2 Key M Connector (SCN2)

The SCN2 is a M.2 2280 Key M connector supporting PCIe 4.0 x4 or SATA, recommended for installing storage module.

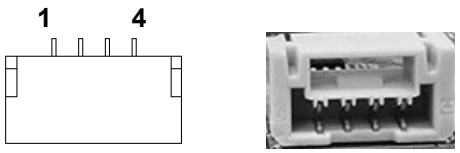
Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	GND	4	+3.3V
5	PCIE_RXN_4	6	NC
7	PCIE_RXP_4	8	NC
9	GND	10	TP1
11	PCIE_TXN_4	12	+3.3V
13	PCIE_TXP_4	14	+3.3V
15	GND	16	+3.3V
17	PCIE_RXN_3	18	+3.3V
19	PCIE_RXP_3	20	NC
21	GND	22	NC
23	PCIE_TXN_3	24	NC
25	PCIE_TXP_3	26	NC
27	GND	28	NC
29	PCIE_RXN_2	30	NC
31	PCIE_RXP_2	32	NC
33	GND	34	NC
35	PCIE_TXN_2	36	NC
37	PCIE_TXP_2	38	NC
39	GND	40	NC
41	PCIE_RXN_1/SATA_RXP	42	NC
43	PCIE_RXP_1/SATA_RXN	44	NC
45	GND	46	NC
47	PCIE_TXN_1/SATA_TXN	48	NC
49	PCIE_TXP_1/SATA_TXP	50	PERST#
51	GND	52	CLKREQ#
53	REF_CLK_N	54	PEWAKE#
55	REF_CLK_P	56	NC
57	GND	58	NC
59	**Key M**	60	**Key M**
61		62	
63		64	
65		66	
67	NC	68	SUSCLK
69	KEYM_PEDET	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	GND		



2.4.14 SMBus Connector (SCN3)

This is a 4-pin (pitch=1.25mm) connector for SMBus interface which is compatible with I²C. It is recommended to use 1.25mm pitch Molex PicoBlade series female connectors for cable assembly. This connector features a snap-on design.

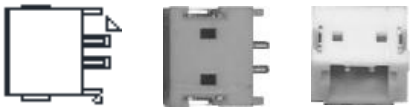
Pin	Signal
1	SMB_CLK_SBY
2	SMB_DAT_SBY
3	SMB_ALERT_N
4	GND



2.4.15 Fan Connector (SCN5)

This is a 2-pin (pitch=1.5mm) wafer connector for 12V/0.5A fan interface.

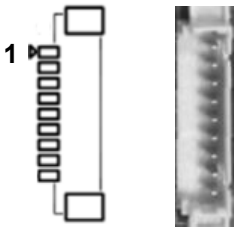
Pin	Signal
1	+V12S
2	GND



2.4.16 COM Connector (SCN6)

This is a 9-pin (pitch=1.25mm) connector which is compliant with Molex 53047-0910. The SCN6 supports RS-232/422/485, selectable via BIOS setting (see section 4.4). The pin assignments for RS-232/422/485 are listed in table below. It is strongly recommended to use the matching cable, 59380880250E.

Pin	RS-232	RS-422	RS-485
1	GND	GND	GND
2	RI1	No use	No use
3	DTR1	RX1-	No use
4	CTS1	No use	No use
5	TX1	RX1+	No use
6	RTS1	No use	No use
7	RX1	TX1+	Data+
8	DSR1	No use	No use
9	DCD1	TX1-	Data-



2.4.17 CMOS Battery Connector (BAT1)

This is a 2-pin (pitch=1.25mm) wafer connector for CMOS battery interface.

Pin	Signal
1	BAT1(+3V level)
2	GND

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Section 3
Hardware Description

3.1 Microprocessors

The PICO570 supports Intel® Core™ Ultra Processors (Series 1) processors which enable your system to operate under Windows® 11/10 and Linux environments. The system performance depends on the microprocessor. Make sure all correct settings are arranged for your installed microprocessor to prevent the CPU from damages.

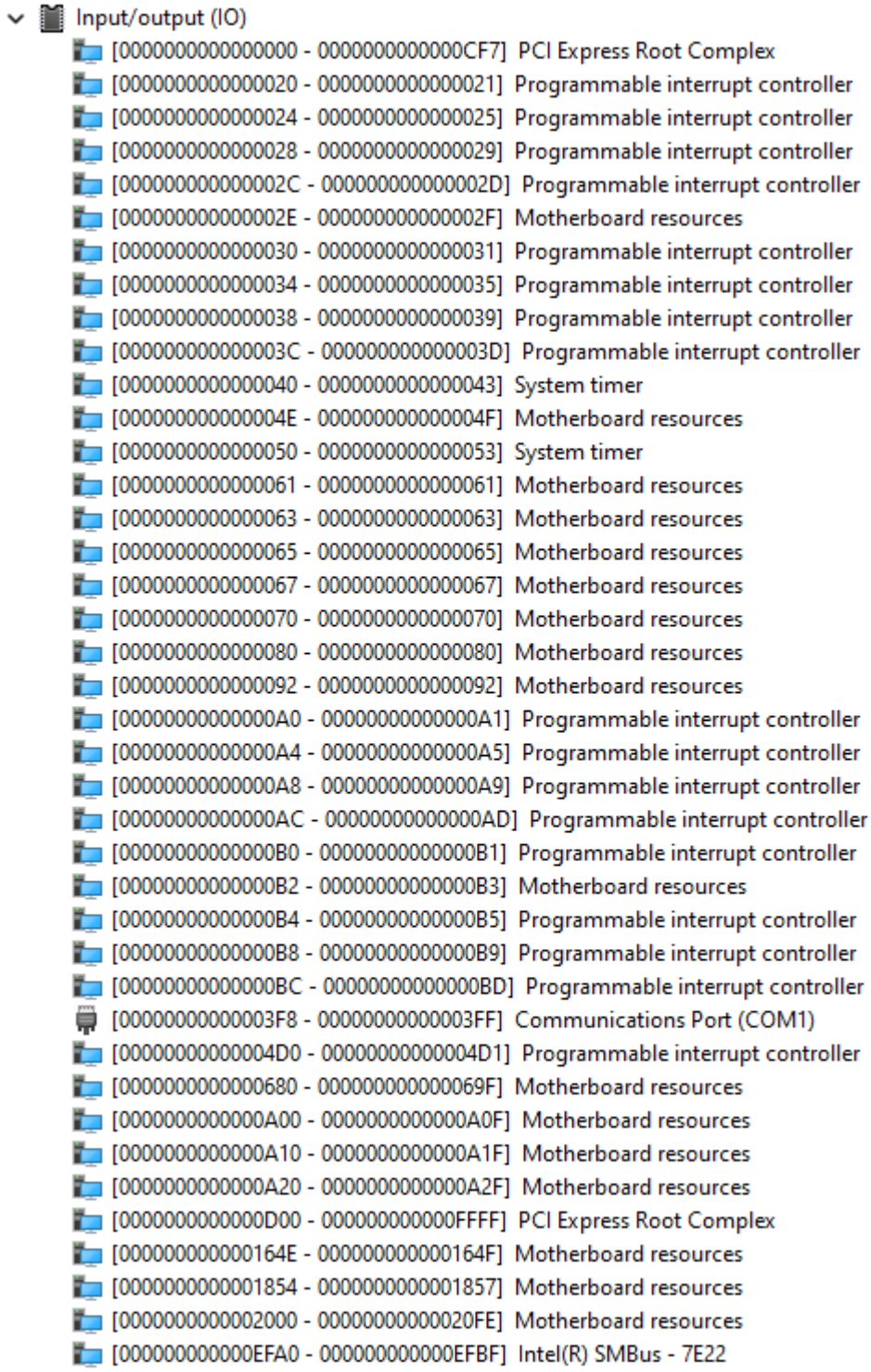
3.2 BIOS

The PICO570 uses AMI Plug and Play BIOS with a single 256Mbit SPI Flash.

3.3 System Memory

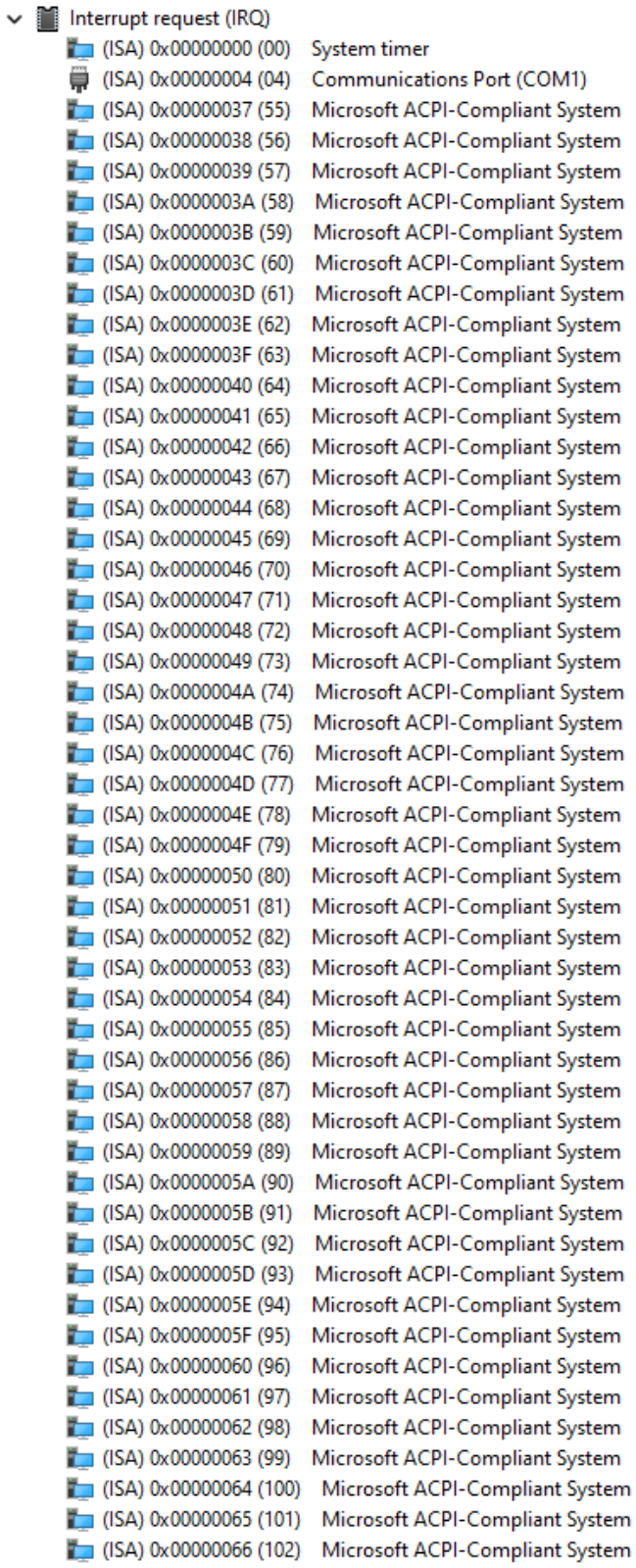
The PICO570 supports one 262-pin DDR5 unbuffered SO-DIMM socket for maximum memory capacity up to 64GB DDR5 SDRAMs. The memory module comes in sizes of 8GB, 16GB, 32GB, 48GB and 64GB.

3.4 I/O Port Address Map



3.5 Interrupt Controller (IRQ) Map

The interrupt controller (IRQ) mapping list is shown as follows:



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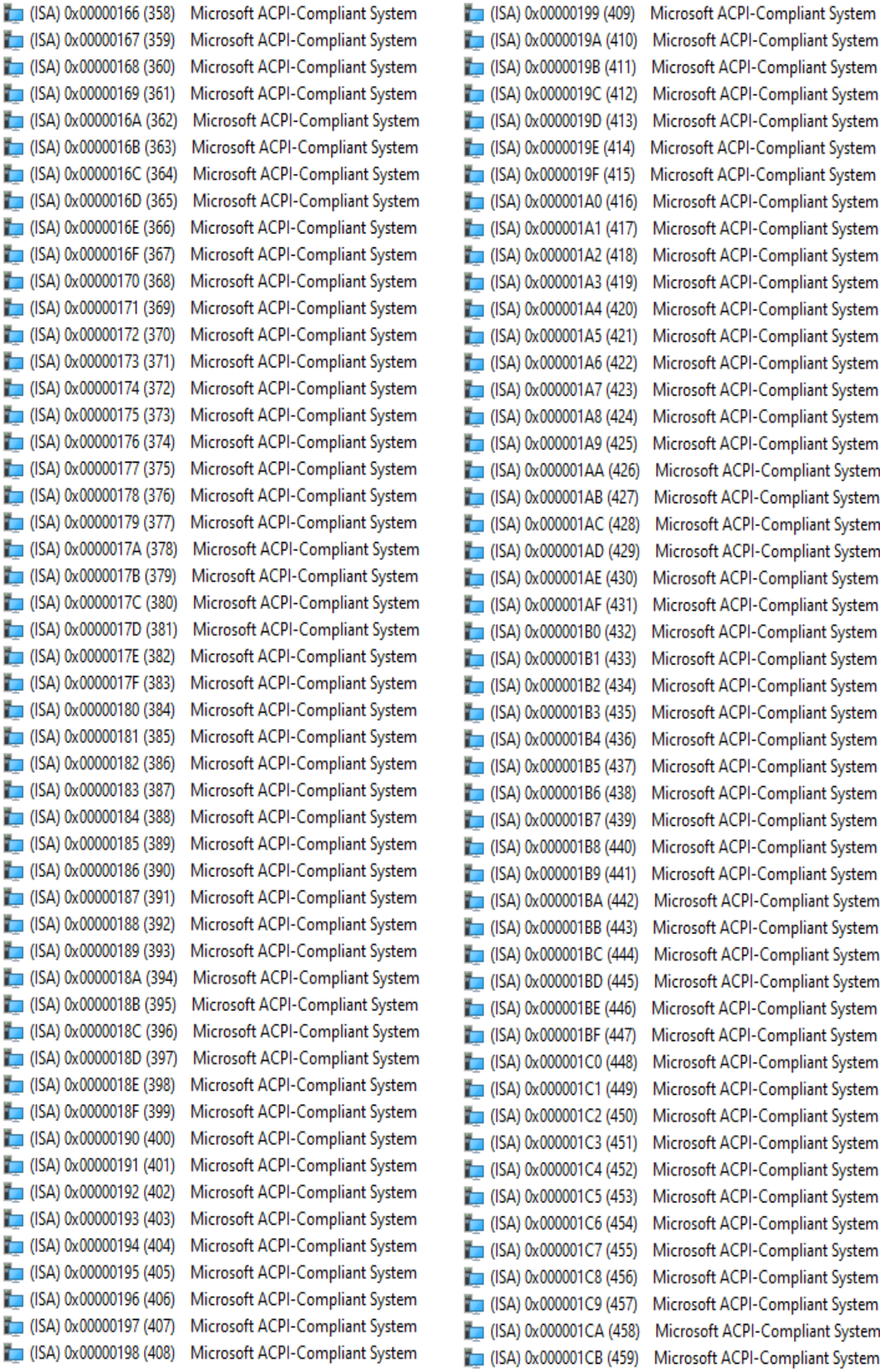
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(ISA) 0x000001C0 (448) Microsoft ACPI-Compliant System
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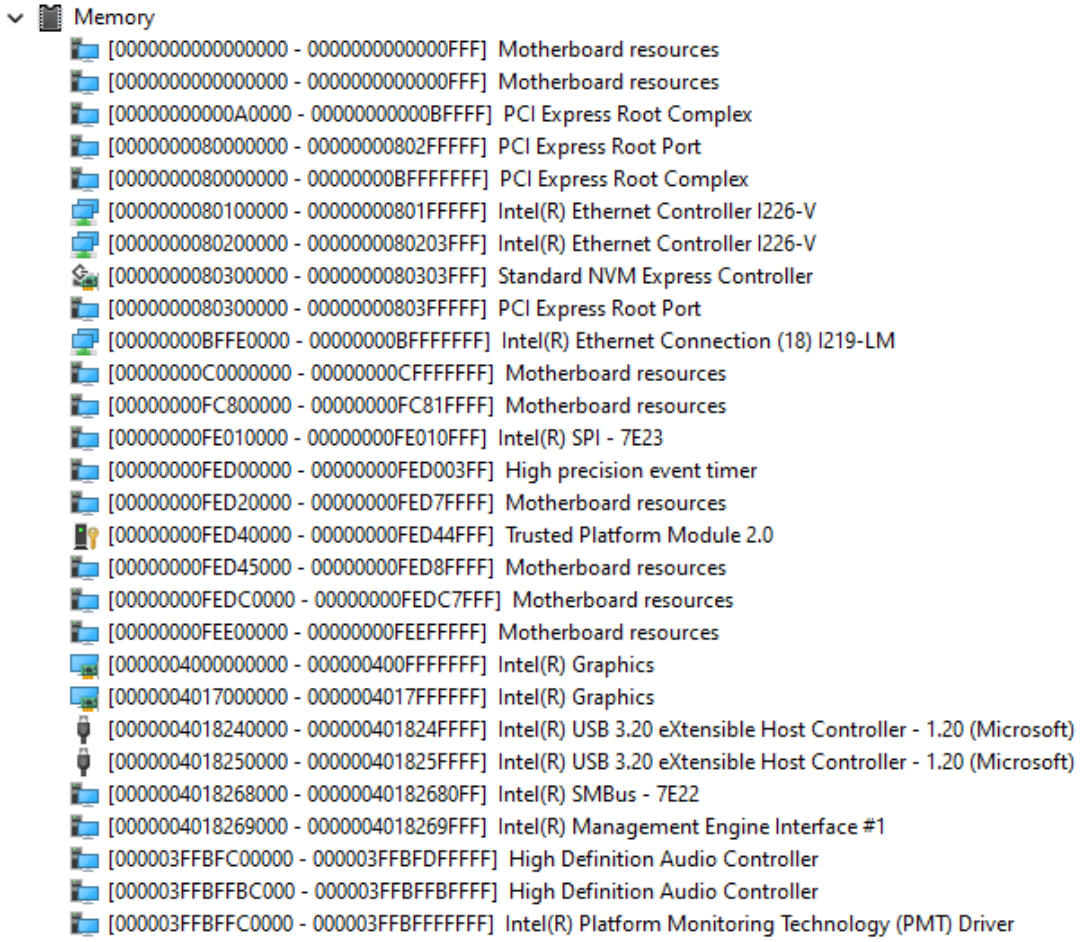
(ISA) 0x000001FC (508) Microsoft ACPI-Compliant System
(ISA) 0x000001FD (509) Microsoft ACPI-Compliant System
(ISA) 0x000001FE (510) Microsoft ACPI-Compliant System

(ISA) 0x000001FF (511) Microsoft ACPI-Compliant System
(PCI) 0x00000010 (16) High Definition Audio Controller
(PCI) 0xFFFFFFE4 (-28) Intel(R) Ethernet Connection (18) I219-LM
(PCI) 0xFFFFFFE5 (-27) Intel(R) Graphics
(PCI) 0xFFFFFFE6 (-26) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFE7 (-25) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFE8 (-24) Intel(R) Management Engine Interface #1
(PCI) 0xFFFFFFE9 (-23) Intel(R) Ethernet Controller I226-V
(PCI) 0xFFFFFFEA (-22) Intel(R) Ethernet Controller I226-V
(PCI) 0xFFFFFFEB (-21) Intel(R) Ethernet Controller I226-V
(PCI) 0xFFFFFFEC (-20) Intel(R) Ethernet Controller I226-V
(PCI) 0xFFFFFFED (-19) Intel(R) Ethernet Controller I226-V
(PCI) 0xFFFFFFEE (-18) Standard NVM Express Controller
(PCI) 0xFFFFFFEF (-17) Standard NVM Express Controller
(PCI) 0xFFFFFFF0 (-16) Standard NVM Express Controller
(PCI) 0xFFFFFFF1 (-15) Standard NVM Express Controller
(PCI) 0xFFFFFFF2 (-14) Standard NVM Express Controller
(PCI) 0xFFFFFFF3 (-13) Standard NVM Express Controller
(PCI) 0xFFFFFFF4 (-12) Standard NVM Express Controller
(PCI) 0xFFFFFFF5 (-11) Standard NVM Express Controller
(PCI) 0xFFFFFFF6 (-10) Standard NVM Express Controller
(PCI) 0xFFFFFFF7 (-9) Standard NVM Express Controller
(PCI) 0xFFFFFFF8 (-8) Standard NVM Express Controller
(PCI) 0xFFFFFFF9 (-7) Standard NVM Express Controller
(PCI) 0xFFFFFFFA (-6) Standard NVM Express Controller
(PCI) 0xFFFFFFFB (-5) Standard NVM Express Controller
(PCI) 0xFFFFFFFC (-4) Standard NVM Express Controller
(PCI) 0xFFFFFFFD (-3) PCI Express Root Port
(PCI) 0xFFFFFFFE (-2) PCI Express Root Port

3.6 Memory Map

The memory mapping list is shown as follows:



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Section 4
AMI BIOS Setup Utility

The AMI UEFI BIOS provides users with a built-in setup program to modify basic system configuration. All configured parameters are stored in a flash chip to save the setup information whenever the power is turned off. This section provides users with detailed description about how to set up basic system configuration through the AMI BIOS setup utility.

4.1 Starting

To enter the setup screens, follow the steps below:

1. Turn on the computer and press the <Del> key immediately.
2. After you press the <Del> key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Advanced and Chipset menus.

Note

If your computer cannot boot after making and saving system changes with BIOS setup, you can restore BIOS optimal defaults by setting SW1 (see section 2.3.2).

It is strongly recommended that you should avoid changing the chipset's defaults. Both AMI and your system manufacturer have carefully set up these defaults that provide the best performance and reliability.

4.2 Navigation Keys

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F2>, <Enter>, <ESC>, <Arrow> keys, and so on.

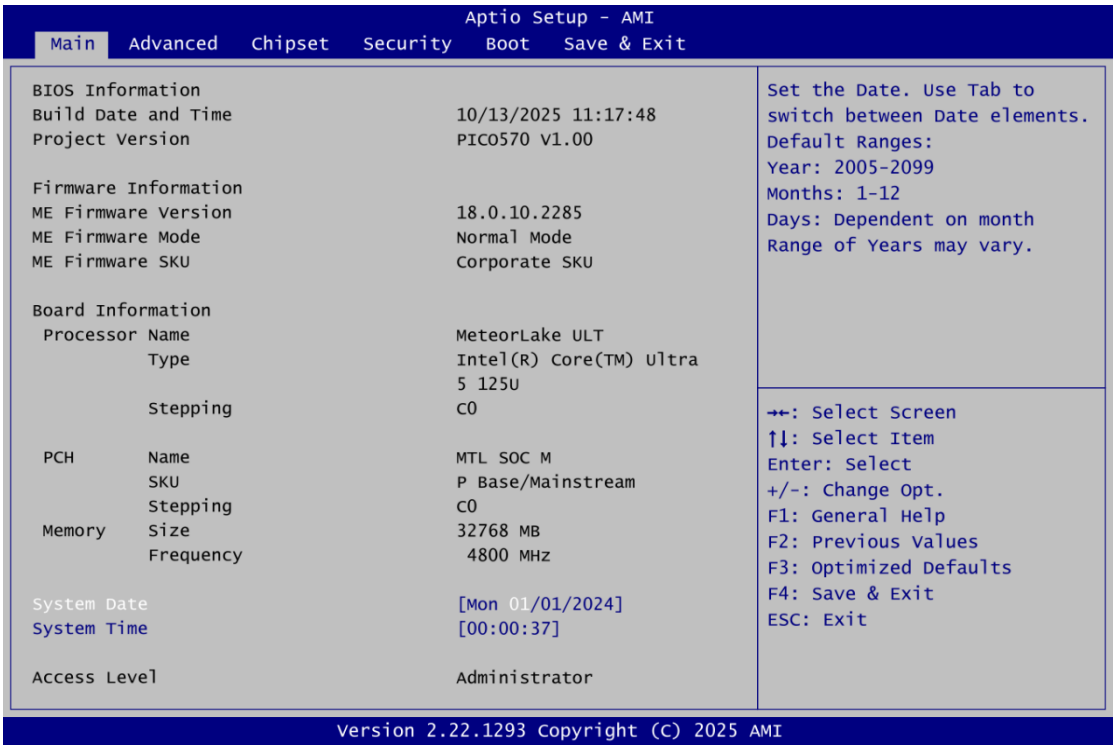
Note

Some of the navigation keys differ from one screen to another.

Hot Keys	Description
→← **Left/Right**	The Left and Right <Arrow> keys allow you to select a setup screen.
↑↓ **Up/Down**	The Up and Down <Arrow> keys allow you to select a setup screen or sub-screen.
+– Plus/Minus	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item.
Tab	The <Tab> key allows you to select setup fields.
F1	The <F1> key allows you to display the General Help screen.
F2	The <F2> key allows you to Load Previous Values.
F3	The <F3> key allows you to Load Optimized Defaults.
F4	The <F4> key allows you to save any changes you have made and exit Setup. Press the <F4> key to save your changes.
Esc	The <Esc> key allows you to discard any changes you have made and exit the Setup. Press the <Esc> key to exit the setup without saving your changes.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub- screens.

4.3 Main Menu

When you first enter the setup utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. System Time/Date can be set up as described below. The Main BIOS setup screen is shown below.



- **BIOS/Firmware/Board Information**
  Display BIOS, firmware and board information.

- **System Date/Time**
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

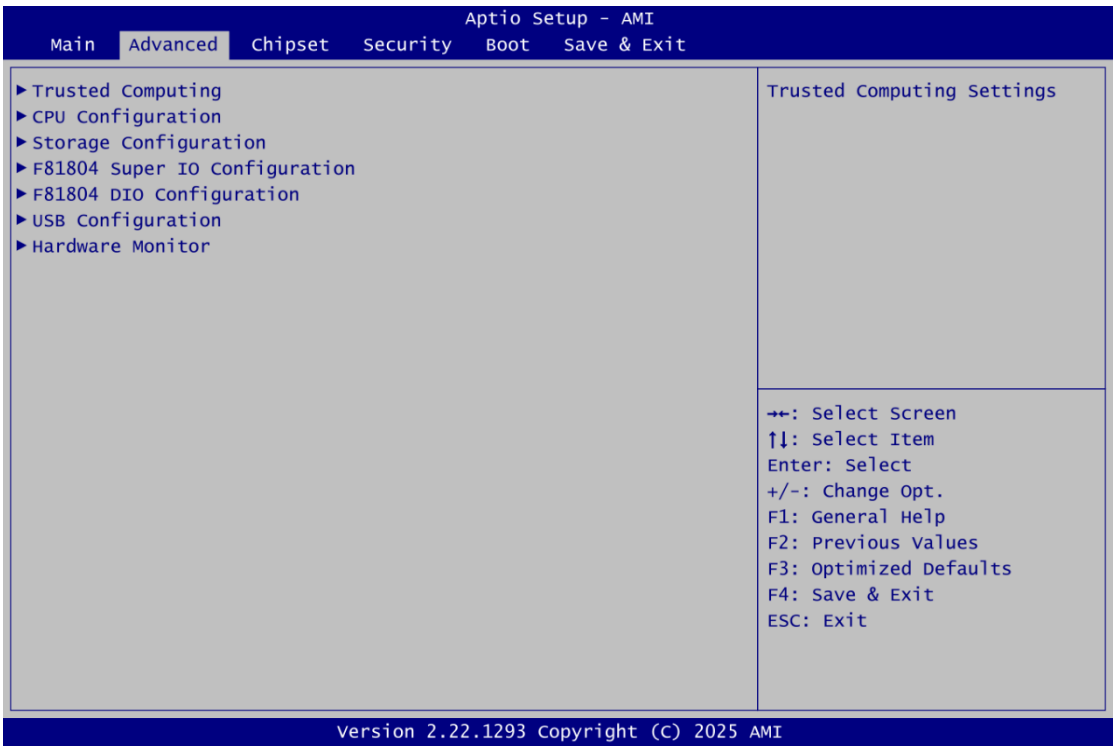
- **Access Level**
  Display the access level of current user.

4.4 Advanced Menu

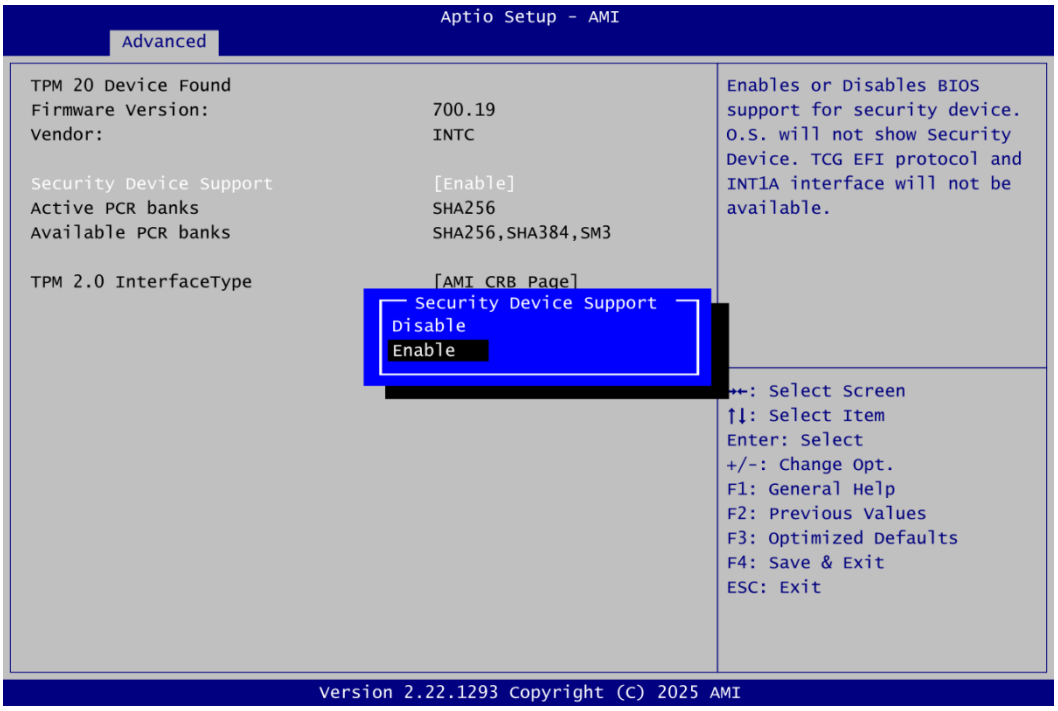
The Advanced menu also allows users to set configuration of the CPU and other system devices. You can select any of the items in the left frame of the screen to go to the sub menus:

- ▶ Trusted Computing
- ▶ CPU Configuration
- ▶ Storage Configuration
- ▶ F81804 Super IO Configuration
- ▶ F81804 DIO Configuration
- ▶ USB Configuration
- ▶ Hardware Monitor

For items marked with "▶", please press <Enter> for more options.

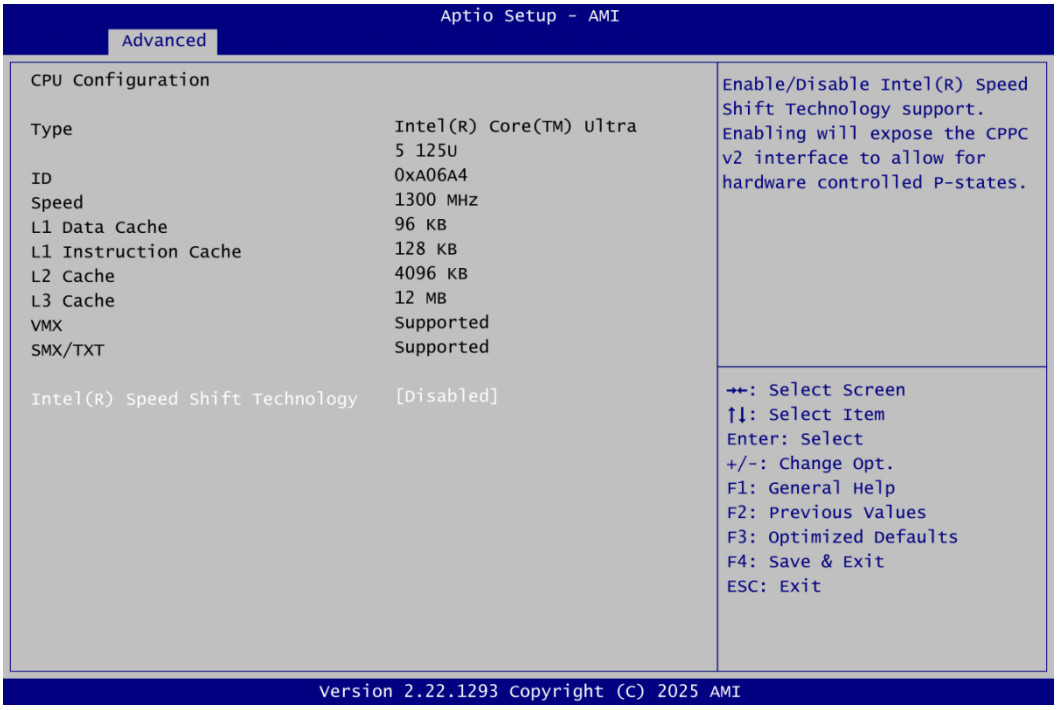


- **Trusted Computing**
  This screen provides function for specifying the TPM settings.

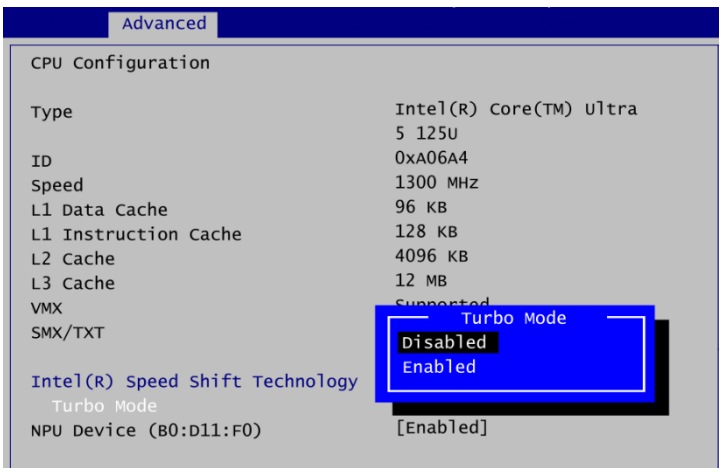


Security Device Support
Enable or disable BIOS support for security device, typically a TPM. When enabled (default setting), the BIOS initializes and makes the TPM available for use by the operating system and other system components. When disabled, the TPM is effectively hidden from the OS, and critical security functions, such as secure boot and disk encryption, may not function. Additionally, TCG EFI protocols and the INT1A interface, which are used for secure boot and other trusted computing tasks, will not be available.

- **CPU Configuration**
  This screen shows the CPU Configuration and you can change the value of the selected option.

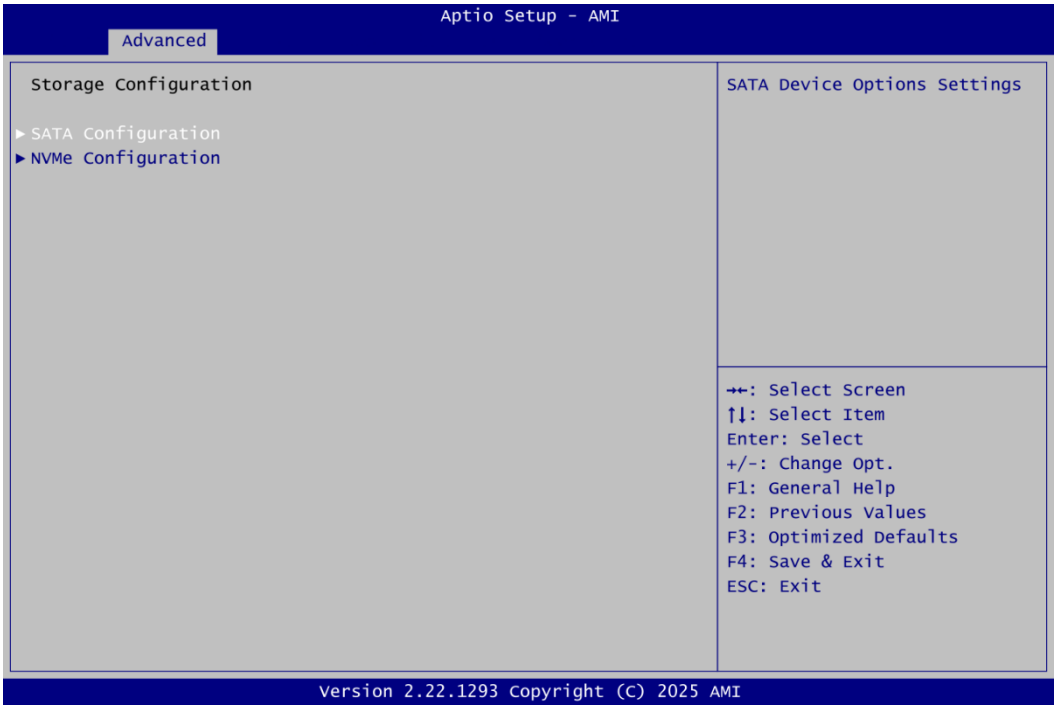


Intel(R) Speed Shift Technology
Enable or disable Intel(R) Speed Shift Technology support. Enabling will trigger the CPPC v2 (Collaborative Processor Performance Control version 2) interface to optimize CPU performance and power management. CPPC works by dynamically adjusting the processor's frequency and voltage in collaboration with the operating system. This helps achieve a balance between performance and energy efficiency.



Turbo Mode
Enable or disable Intel® turbo boost mode allowing processor cores to run faster but not exceed CPU defined frequency limits.

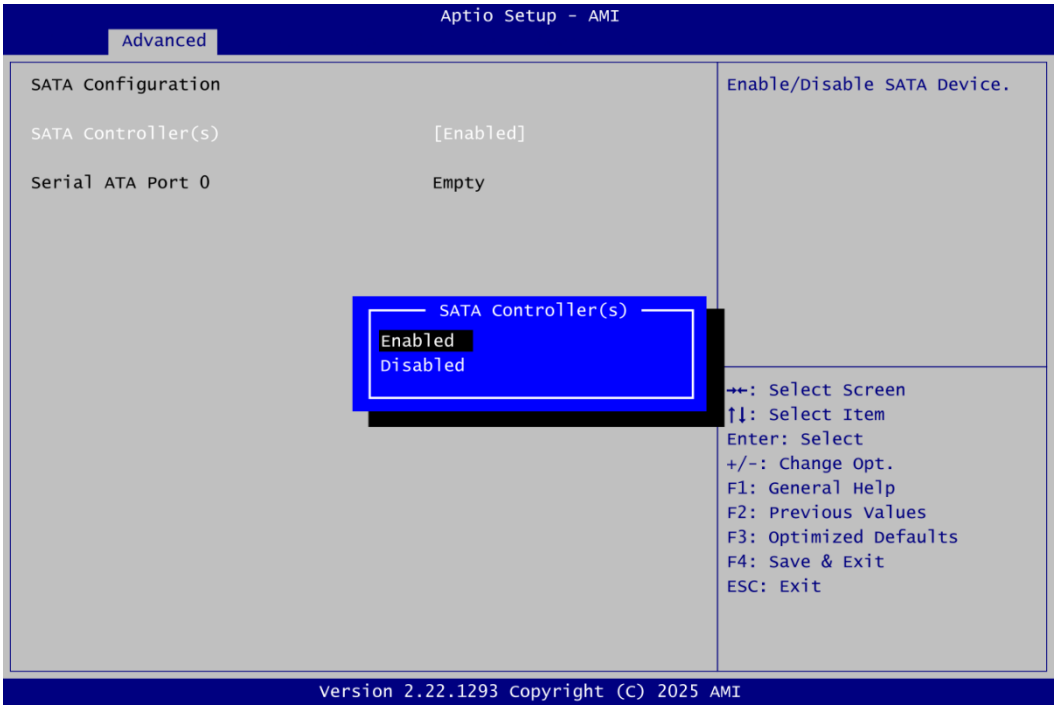
- **Storage Configuration**
  In the Storage Configuration menu, you can see the currently installed hardware in the SCN2 (see section 2.4.13). During system boot up, the BIOS automatically detects the presence of installed devices.



SATA Configuration
Click to open SATA device setting sub-screen.

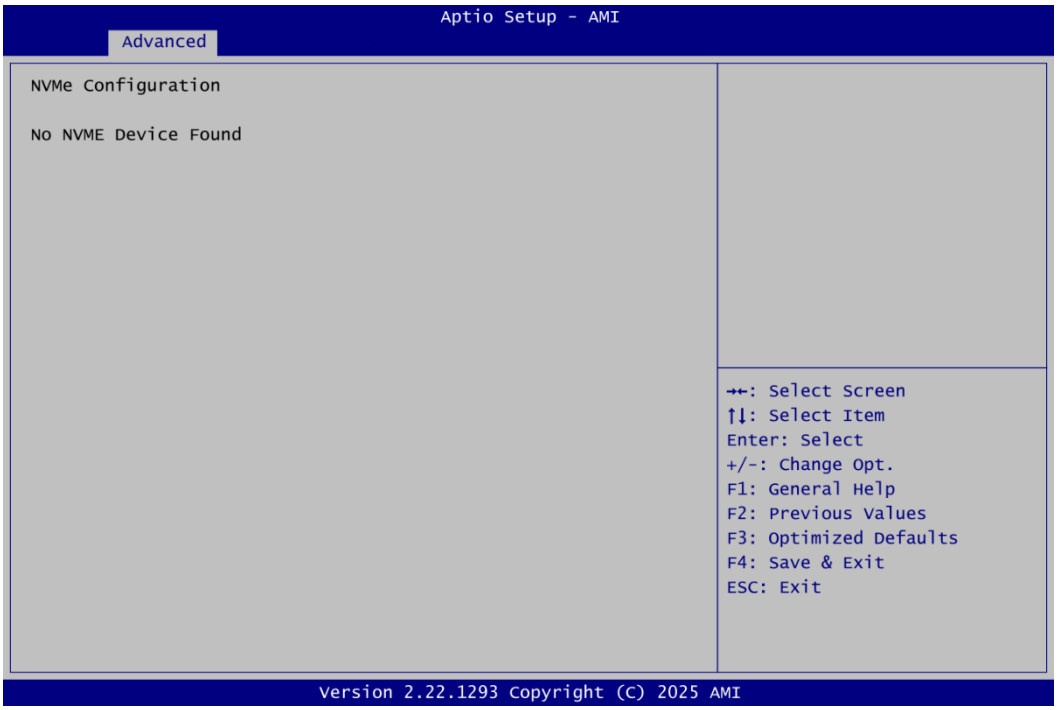
NVMe Configuration
Click to open NVMe (Non-Volatile Memory Express) storage device related information and setting sub-screen.

SATA Configuration

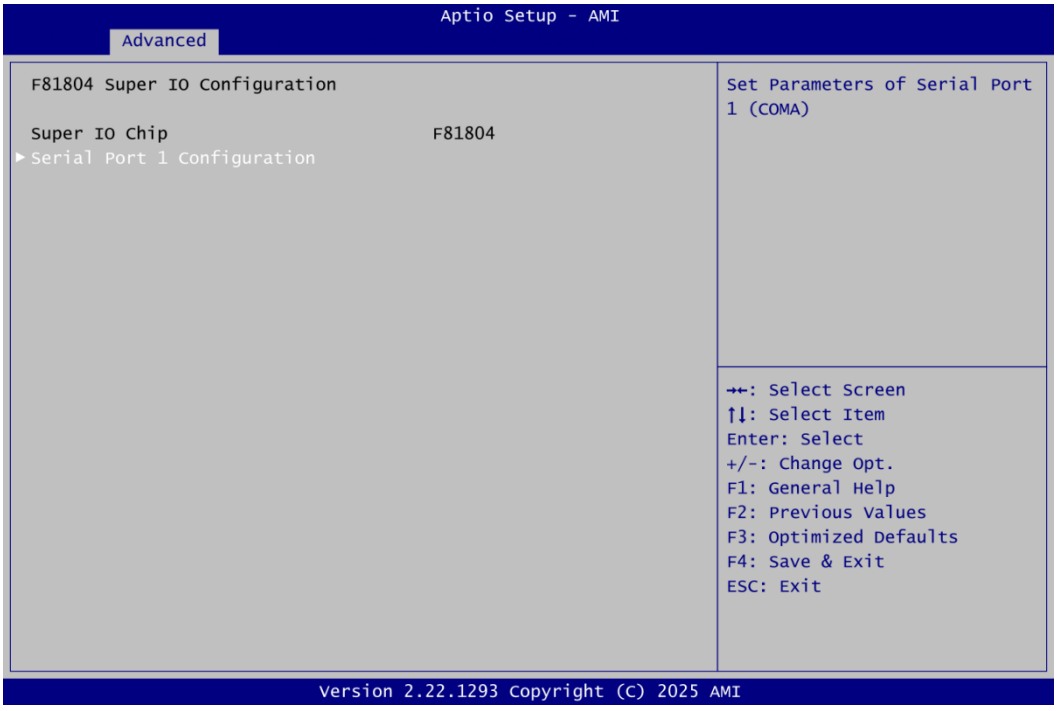


SATA Controller(s)
Enable or disable the SATA Controller feature.

NVMe Configuration

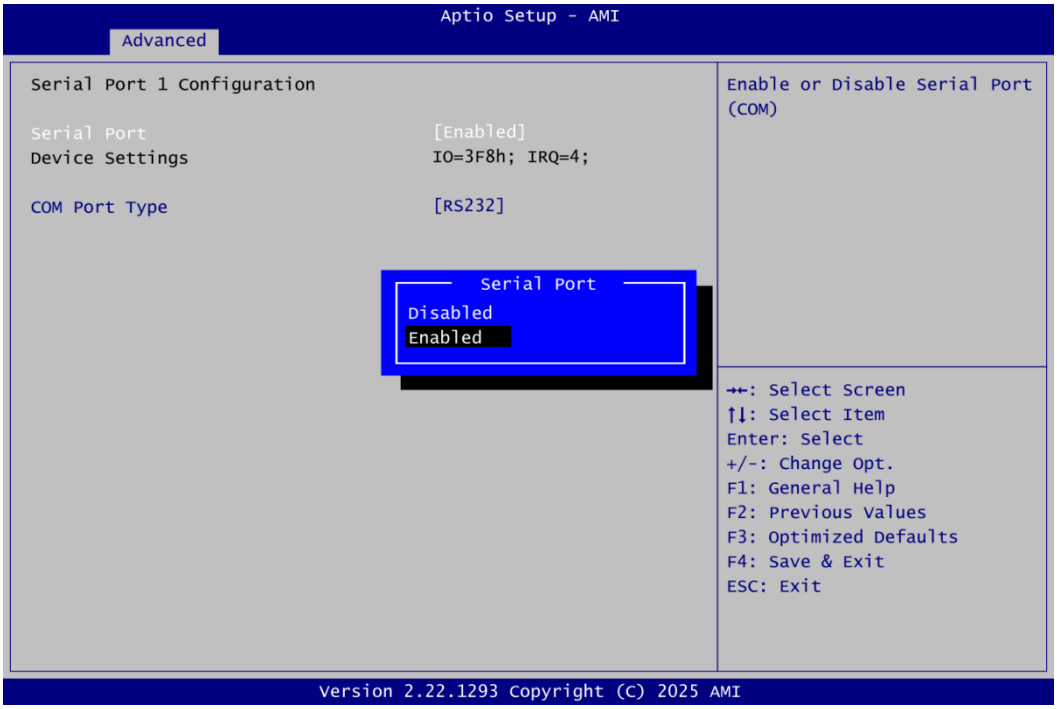


- **F81804 Super IO Configuration**
  You can use this screen to select options for Serial Port configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen. For items marked with "▶", please press <Enter> for more options.

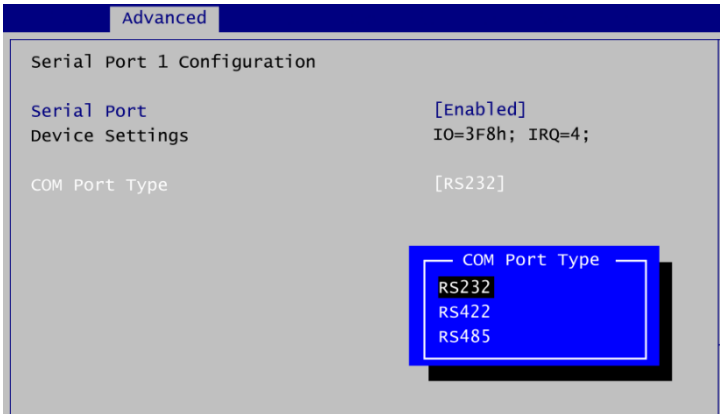


Serial Port 1 Configuration
Use these items to set parameters related to serial port 1.

- **Serial Port 1 Configuration**

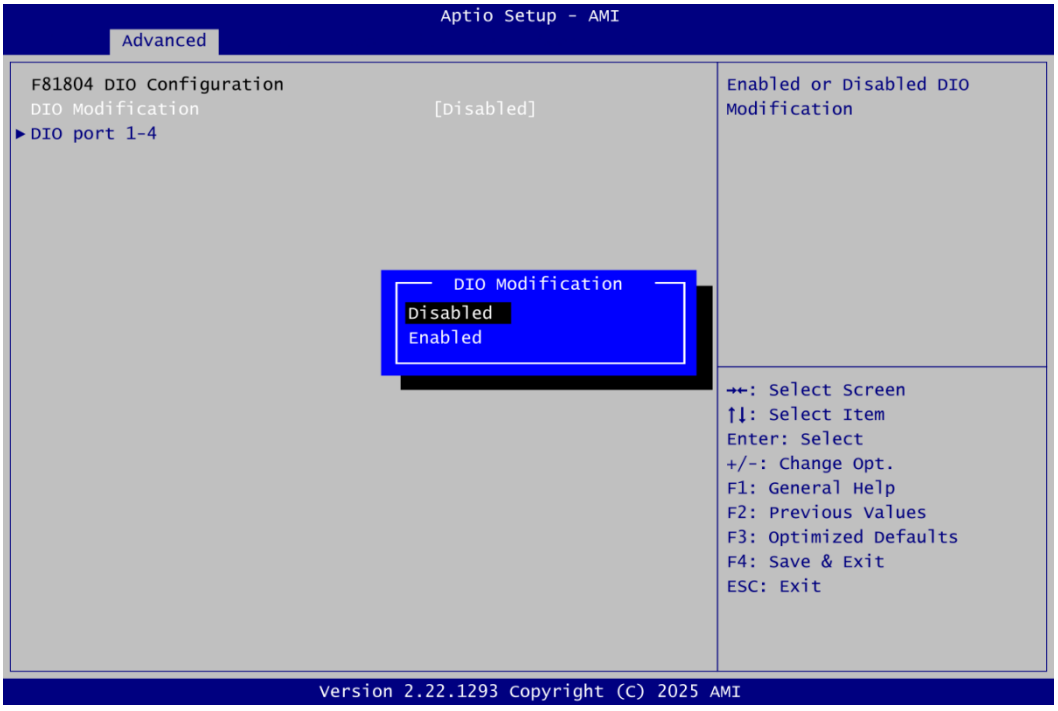


Serial Port
Enable or disable serial port 1. The optimal setting for base I/O address is 3F8h and for interrupt request address is IRQ4.

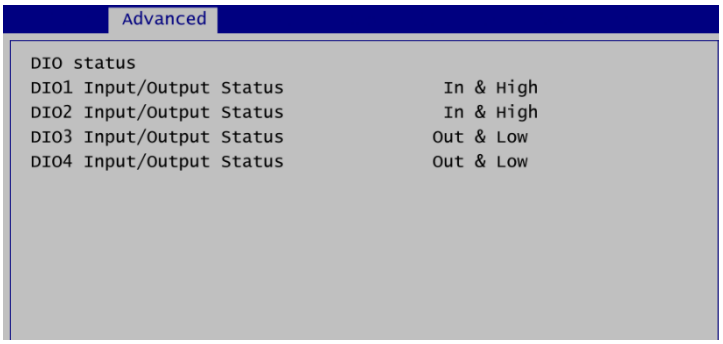


COM Port Type
Use this item to set RS-232/422/485 communication mode.

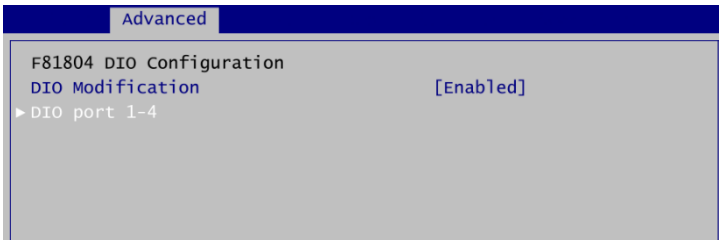
- **F81804 DIO Configuration**
  You can use this screen to select options for the 4-bit Digital I/O Configuration. A description of selected item appears on the right side of the screen. For items marked with "▶", please press <Enter> for more options.



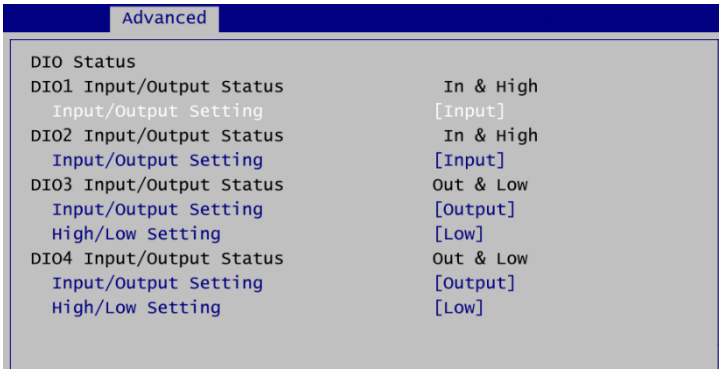
DIO Modification
This setting controls whether the digital I/O (DIO) status can be modified through the system interface.
When set to Disabled, the DIO configuration remains in a read-only mode — meaning the interface only displays the current DIO status without allowing any modifications. The DIO status sub screen is as follows:



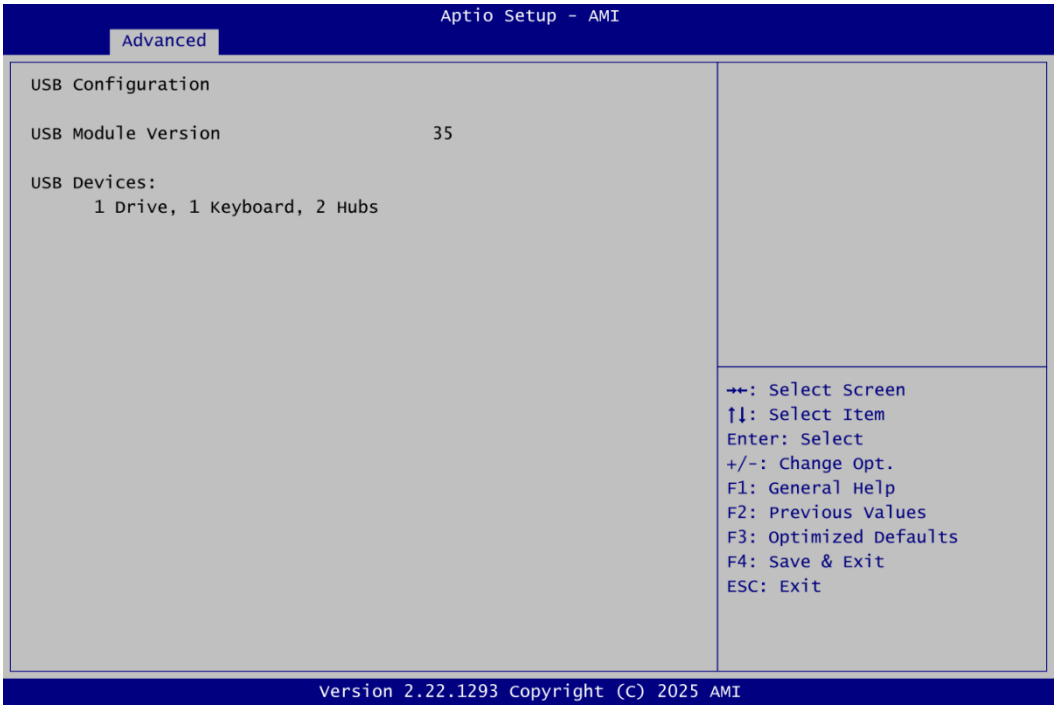
If DIO Modification is enabled, you can be access to the DIO status sub screen to actively change the state of each DIO channel.



DIO port 1-4
Click on this option to open DIO status sub-screen.

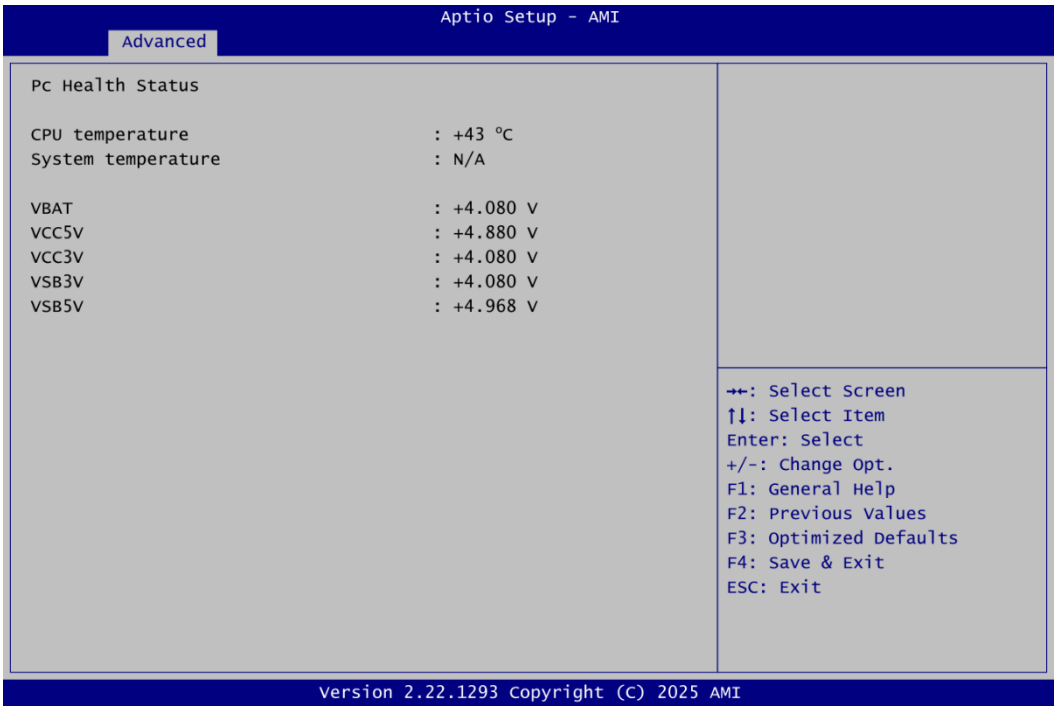


- **USB Configuration**



USB Devices
Display all detected USB devices.

- **Hardware Monitor**
  This screen monitors hardware health status.



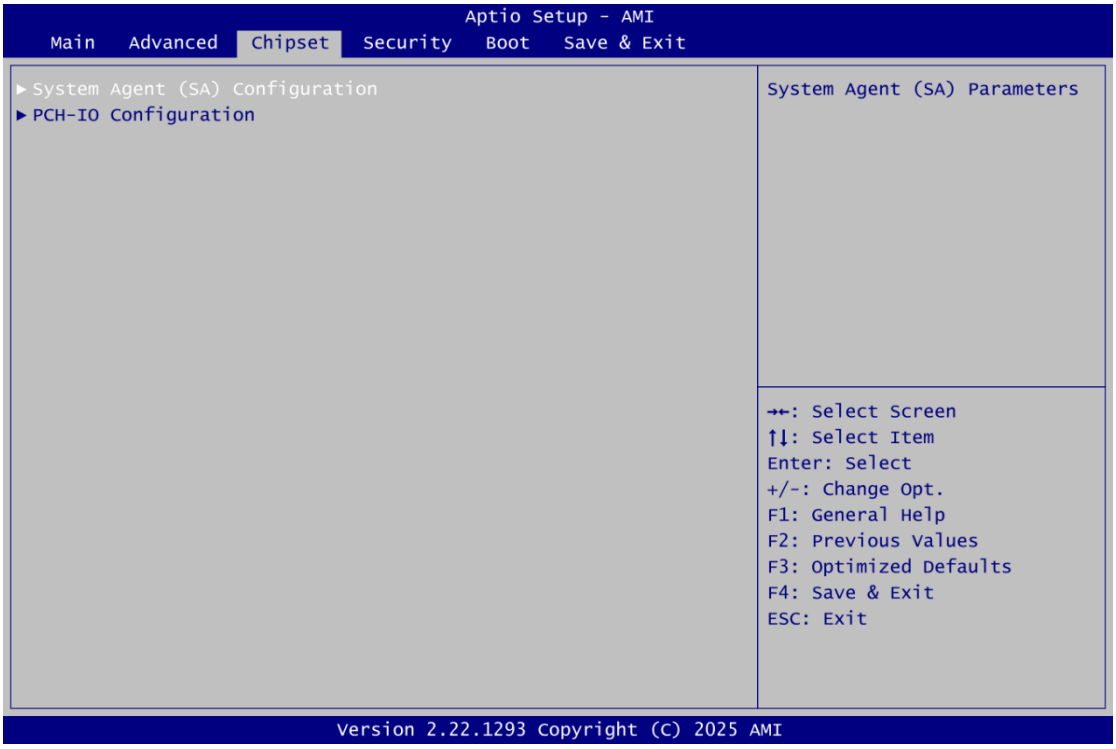
This screen displays the temperature of system and CPU, system voltages (VBAT, VCC5V, VCC3V, VSB3V and VSB5V).

4.5 Chipset Menu

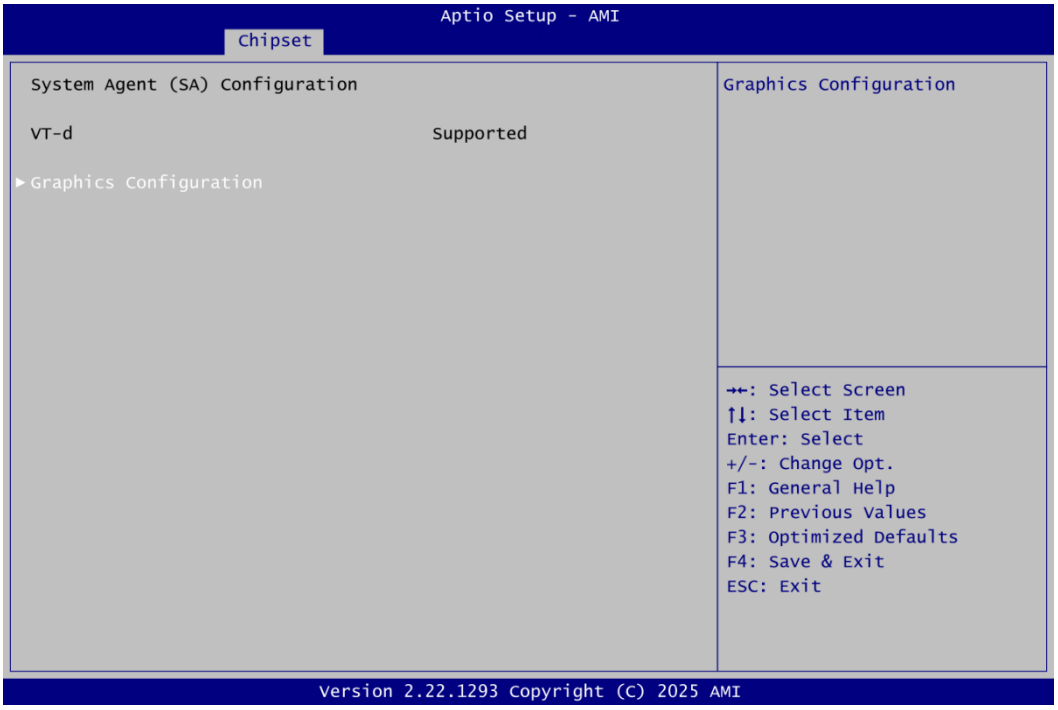
The Chipset menu allows users to change the advanced chipset settings. You can select any of the items in the left frame of the screen to go to the sub menus:

- ► System Agent (SA) Configuration
- ► PCH-IO Configuration

For items marked with "►", please press <Enter> for more options.

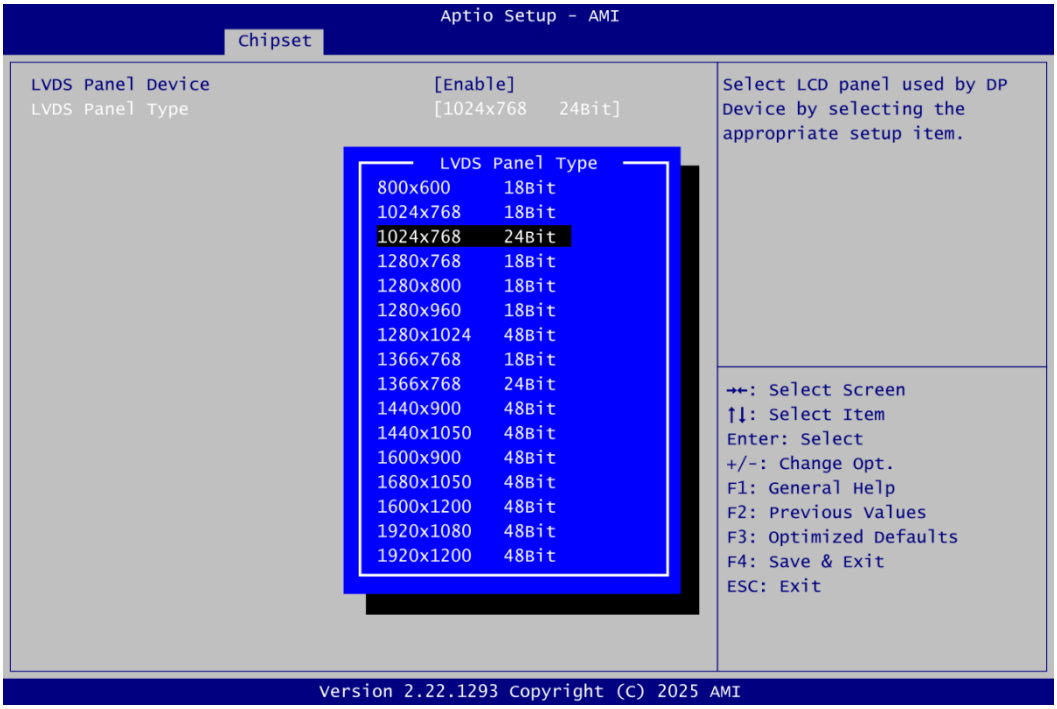


- **System Agent (SA) Configuration**
  This screen allows users to configure System Agent (SA) parameters. For items marked with "►", please press <Enter> for more options.



Graphics Configuration
Open sub menu for parameters related to graphics configuration.

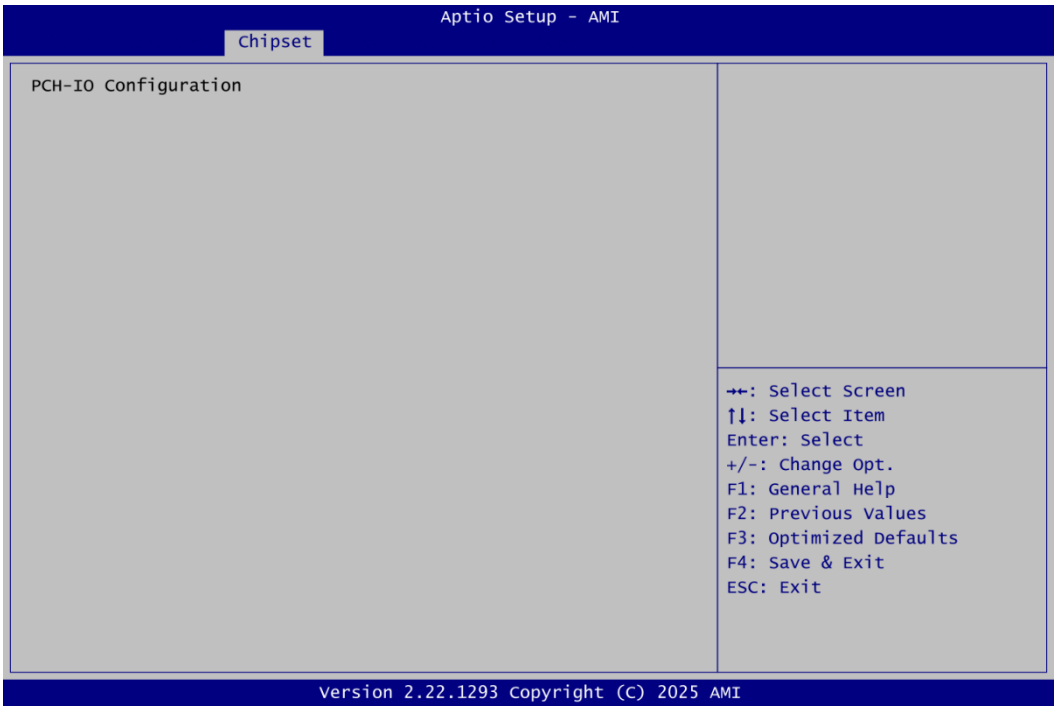
Graphics Configuration



LVDS Panel Device
Enable or disable LVDS panel support.

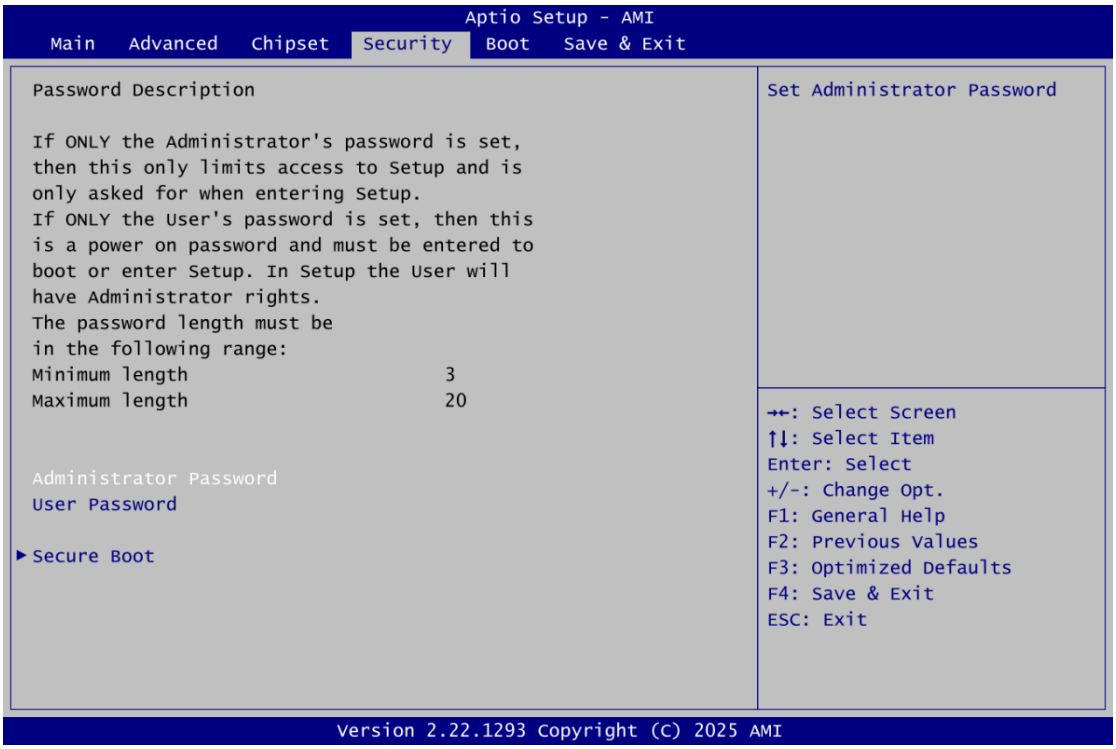
LVDS Panel Type
Select the appropriate LVDS panel resolution.

PCH-IO Configuration
This item is reserved for future adding items.



4.6 Security Menu

The Security menu allows users to change the security settings for the system.

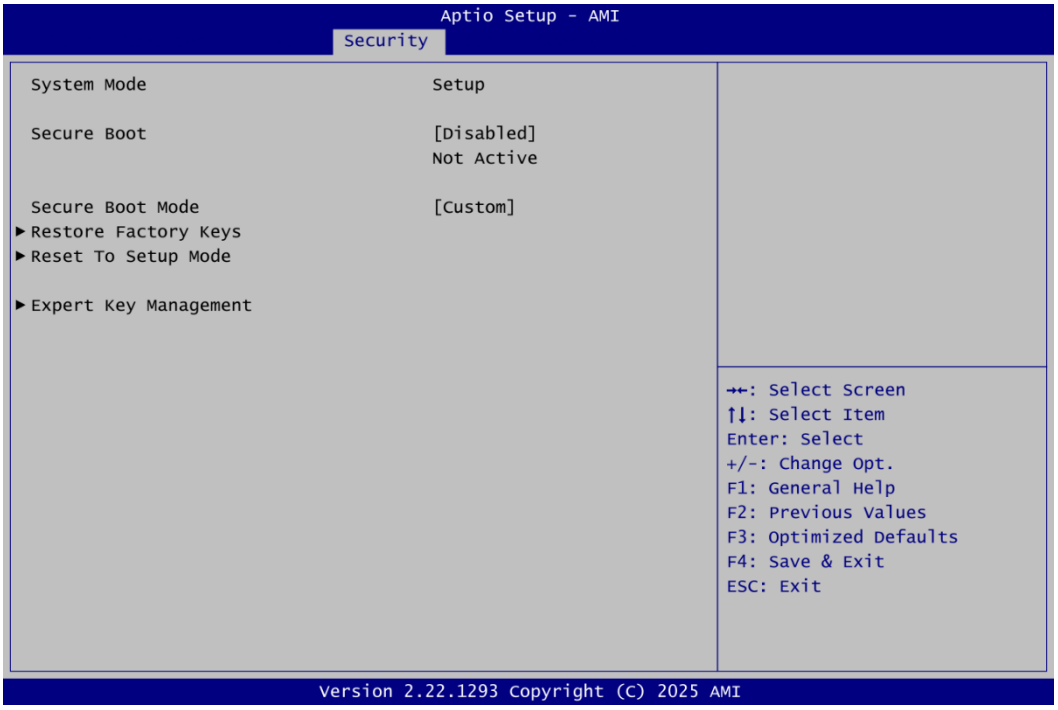


- **Administrator Password**
  Set administrator password.

- **User Password**
  Set user password.

- **Secure Boot**
  Use this item to set parameters related to Secure Boot.

- **Secure Boot**
  The Secure Boot feature is designed to ensure and protect the system from unauthorized access and malwares during boot-up.



Secure Boot
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset. Secure Boot ensures that the system only boots from trusted software, preventing malicious software from loading and compromising the device. It checks the digital signatures of boot loaders, firmware, and operating systems to verify that they are from trusted sources and have not been tampered with. Users can choose to enable it or not, between standard and custom mode.

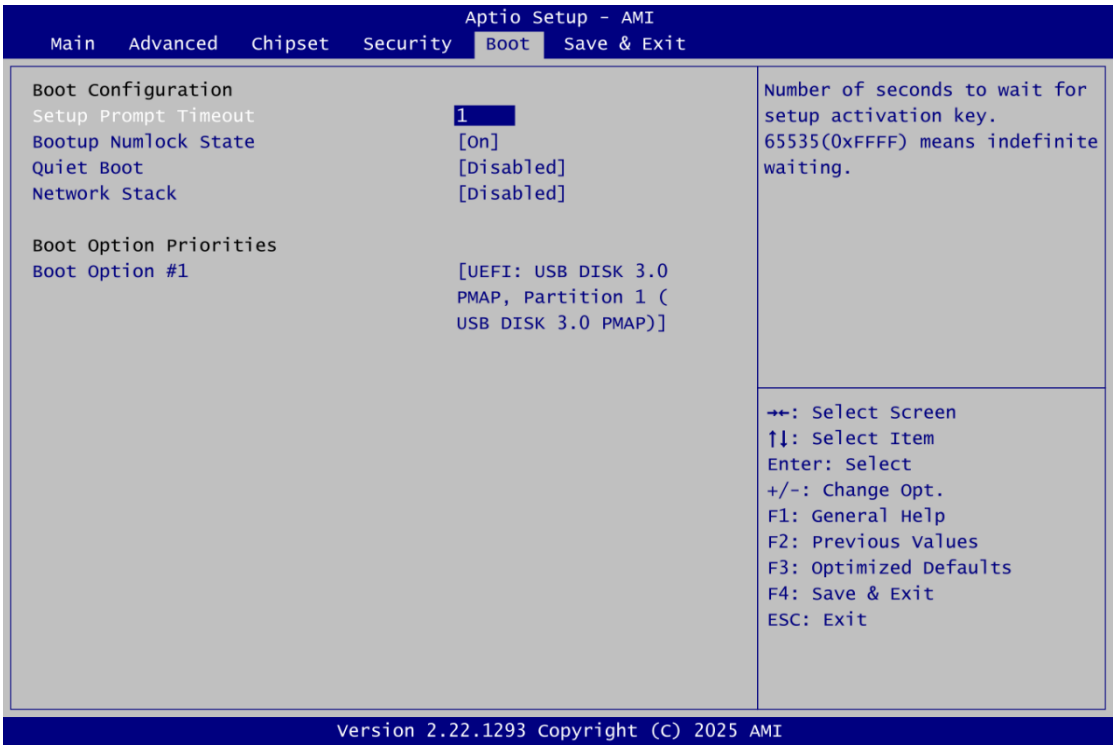
Secure Boot Mode
Secure Boot mode options: Standard or Custom. In Custom mode, the policy of Secure Boot variables can be configured by a physically present user without full authentication.

Restore Factory Keys
Force System to User mode. Install factory default Secure Boot key databases.

Key Management
Enables expert users to modify Secure Boot Policy variables without full authentication.

4.7 Boot Menu

The Boot menu allows users to change boot options of the system.



- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

- **Bootup Numlock State**
  Use this item to select the power-on state for the keyboard NumLock.

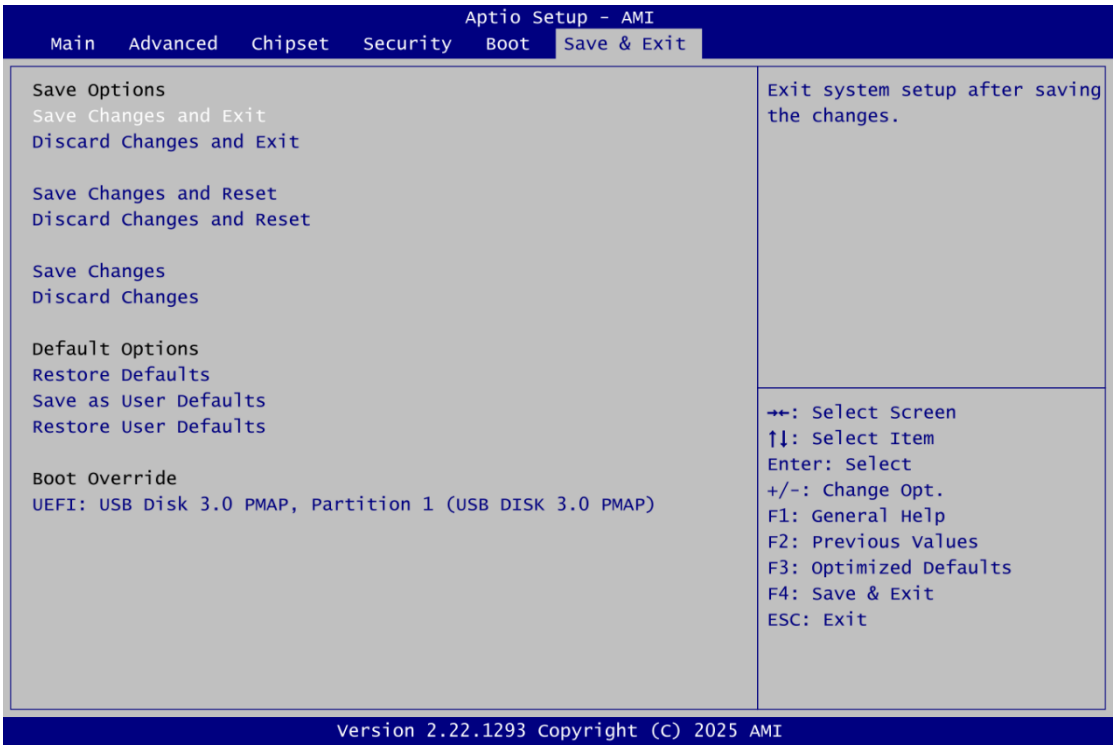
- **Quiet Boot**
  Select to display either POST output messages or a splash screen during boot-up.

- **Network Stack**
  Enable or disable UEFI Network stack.

- **Boot Option Priorities [Boot Option #1, …]**
  These are settings for boot priority. Specify the boot device priority sequence from the available devices.

4.8 Save & Exit Menu

The Save & Exit menu allows users to load your system configuration with optimal or fail-safe default values.



- **Save Changes and Exit**
  When you have completed the system configuration changes, select this option to leave Setup and return to Main Menu. Select Save Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to save changes and exit.

- **Discard Changes and Exit**
  Select this option to quit Setup without making any permanent changes to the system configuration and return to Main Menu. Select Discard Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to discard changes and exit.

- **Save Changes and Reset**
  When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Save Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to save changes and reset.

- **Discard Changes and Reset**
  Select this option to quit Setup without making any permanent changes to the system configuration and reboot the computer. Select Discard Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to discard changes and reset.

- **Save Changes**
  When you have completed the system configuration changes, select this option to save changes. Select Save Changes from the Save & Exit menu and press <Enter>. Select Yes to save changes.

- **Discard Changes**
  Select this option to quit Setup without making any permanent changes to the system configuration. Select Discard Changes from the Save & Exit menu and press <Enter>. Select Yes to discard changes.

- **Restore Defaults**
  It automatically sets all Setup options to a complete set of default settings when you select this option. Select Restore Defaults from the Save & Exit menu and press <Enter>.

- **Save as User Defaults**
  Select this option to save system configuration changes done so far as User Defaults. Select Save as User Defaults from the Save & Exit menu and press <Enter>.

- **Restore User Defaults**
  It automatically sets all Setup options to a complete set of User Defaults when you select this option. Select Restore User Defaults from the Save & Exit menu and press <Enter>.

- **Boot Override**
  Select a drive to immediately boot that device regardless of the current boot order.

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Appendix A
Watchdog Timer

A.1 About Watchdog Timer

After the system stops working for a while, it can be auto-reset by the watchdog timer. The integrated watchdog timer can be set up in the system reset mode by program.

A.2 How to Use Watchdog Timer

Note

Please check Axiomtek eAPI3.0 SDK before using below sample codes.

```
//=============================================================================
//      includes
//=============================================================================

#include <stdio.h>
#include <stdlib.h>
#include <stdint.h>
#include "EApi.h"

#if defined(WIN32) || defined(_WIN32) || defined(__WIN32__) || defined(__NT__)
      #include <Windows.h>
      #include <iostream>
      #define scndata scanf_s
using namespace std;
#else
#define scndata scanf
#endif
unsigned int EapiStatus;

// ****************************************
// Watch Dog
// ****************************************
void WDT_demo()
{
            uint32_t wdt_runmode = 0;
            uint32_t wdt_timermode = 0;
            uint32_t wdt_event = 0;       // run wdt
            uint32_t wdt_delay = 0;       // run wdt
            uint32_t wdt_reset = 0;       // reload wdt

            while (wdt_runmode != 5) {
                        fprintf(stderr, "1. Run WDT \n");
                        fprintf(stderr, "2. Get WDT cap\n");
                        fprintf(stderr, "3. Reload WDT \n");
                        fprintf(stderr, "4. Stop WDT \n");
```

```
                fprintf(stderr, "5. Exit\n");
                fprintf(stderr, "Select WDT mode: ");
                scndata("%d", &wdt_runmode);

                switch (wdt_runmode)
                {
                case 1:
                        fprintf(stderr, "Set WDT timer mode (0 means second, 1 means
minute):");
                        scndata("%d", &wdt_timermode);

                        if (wdt_timermode == 0)
                        {
                                fprintf(stderr, "WDT timer mode is second.\n");
                        }
                        else if (wdt_timermode == 1)
                        {
                                fprintf(stderr, "WDT timer mode is minute.\n");
                        }
                        else
                        {
                                wdt_timermode = 0;
                                fprintf(stderr, "WDT timer mode is second.\n");
                        }

                        fprintf(stderr, "Set WDT wdt_delay: ");
                        scndata("%d", &wdt_delay);

                        fprintf(stderr, "Set WDT wdt_event : ");
                        scndata("%d", &wdt_event );

                        fprintf(stderr, "Set WDT wdt_reset :");
                        scndata("%d", &wdt_reset);

                        if (wdt_timermode == 0)
                                EapiStatus = EApiWDogStart(wdt_delay * 1000,
wdt_event * 1000, wdt_reset * 1000);
                        else if (wdt_timermode == 1)
                                EapiStatus = EApiWDogStart(wdt_delay * 60000,
wdt_event * 60000, wdt_reset * 60000);

                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Run WDT not support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Run WDT successful.\n\n");
                        }
                        break;
                case 2:
                        EapiStatus = EApiWDogGetCap(&wdt_delay, &wdt_event,
&wdt_reset);
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Get WDT cap not suppor!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Get WDT cap wdt_delay: %d,
wdt_event: %d, wdt_reset:%d \n\n", wdt_delay, wdt_event, wdt_reset);
                        }
                        break;
                case 3:
```

```
                                        EapiStatus = EApiWDogTrigger();
                                                if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                                        fprintf(stderr, "Reload WDT not
support!!!\n\n");
                                                }
                                                else
                                                        fprintf(stderr, "Reload WDT
successful.\n\n");

                                        break;
                                case 4:
                                        EapiStatus = EApiWDogStop();
                                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                                fprintf(stderr, "Stop WDT not support!!!\n\n");
                                        }
                                        else {
                                                fprintf(stderr, "Stop WDT successful.\n\n");
                                        }
                                        break;
                                case 5:
                                        fprintf(stderr, "Exit WDog mode!!!\n\n");
                                        break;
                                default:
                                        fprintf(stderr, "Select error!!!\n\n");
                                        break;
                                }
                                fprintf(stderr, "*****************************************\n");
                        }
}

int main (
        int argc,
        char *argv[]
) {

        //
        // Initialize
        //
        EapiStatus = EApiLibInitialize ();
        if (EapiStatus != EAPI_STATUS_SUCCESS) {
          fprintf (stderr, "Fail to initialize");
        }
        else
        {
          fprintf (stderr, "---- intialize: ok\n");
          WDT_demo();
        }
        return 0;
}
```

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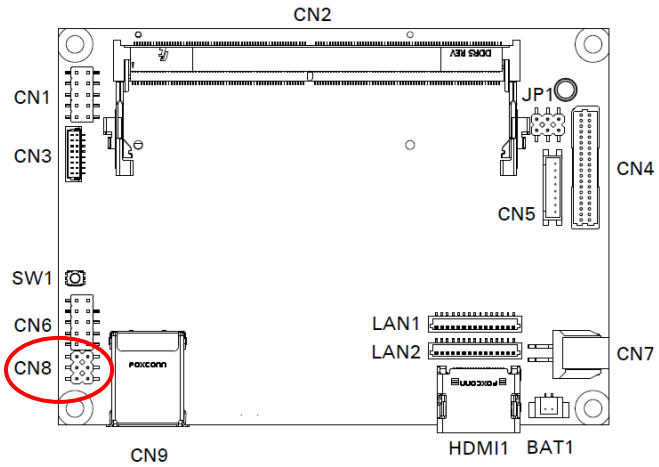
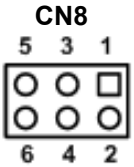
Appendix B
Digital I/O

B.1 About Digital I/O

The onboard GPIO or digital I/O has 4 bits (DIO0~3). Each bit can be set to function as input or output by software programming. In default, all pins are pulled high with +5V level (according to main power). The BIOS default settings are 2 inputs and 2 outputs.





Pin	Signal	Pin	Signal
1	DIO 0	2	DIO 3
3	DIO 1	4	DIO 2
5	+5V	6	GND

B.2 Digital I/O Programming

Note

Please check Axiomtek eAPI3.0 SDK before using below sample codes.

```
#include <stdio.h>
#include <stdlib.h>
#include <stdint.h>
#include "EApi.h"
#if defined(WIN32) || defined(_WIN32) || defined(__WIN32__) || defined(__NT__)
	#include <Windows.h>
	#include <iostream>
	#define scndata scanf_s
using namespace std;

#else

#define scndata scanf

#endif
unsigned int EapiStatus;
// ****************************************
```

```
// Menu
// ****************************************


// ****************************************
// Load and Initilize eAPI library
// ****************************************
int InitLibrary()
{

        return EApiLibInitialize() != EAPI_STATUS_SUCCESS;
}


void GPIO_demo()
{

        uint32_t GPIO_runmode = 0;
        uint32_t ID = 0;
        uint32_t mask = 0;
        uint32_t value = 0;
        uint32_t inmask = 0;


        while (GPIO_runmode != 6) {
            ID = 0;
                mask = 0;
                value = 0;
                inmask = 0;
                fprintf(stderr, "1. Get GPIO DirectionCaps\n");
                fprintf(stderr, "2. Get GPIO Direction\n");
                fprintf(stderr, "3. Set GPIO Direction\n");
                fprintf(stderr, "4. Get GPIO Level\n");
                fprintf(stderr, "5. Set GPIO Level\n");
                fprintf(stderr, "6. Exit\n");
                fprintf(stderr, "Select GPIO run mode: ");
                scndata("%d", &GPIO_runmode);
                switch (GPIO_runmode)
                {
                case 1:
                        fprintf(stderr, "Bank: 0x10000\n");
                        fprintf(stderr, "Enter the ID(hex): ");
                        scndata("%x", &ID);
                        EapiStatus = EApiGPIOGetDirectionCaps(ID, &mask, &value);
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Get GPIO DirectionCaps not
support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Get GPIO DirectionCaps ID: %x,
Inputmask: %x, Outputmask: %x\n\n", ID, mask, value);
                        }
                        break;
                case 2:
                        fprintf(stderr, "Bank: 0x10000\n");
                        fprintf(stderr, "Enter the ID(hex): ");
                        scndata("%x", &ID);
                        fprintf(stderr, "Enter the mask(hex): ");
                        scndata("%x", &mask);
                        EapiStatus = EApiGPIOGetDirection(ID, mask, &value);
```

```
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Get GPIO Direction not
support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Get GPIO Direction ID: %x, mask: %x,
Direction: %x\n\n", ID, mask, value);
                        }
                        break;
                case 3:
                        fprintf(stderr, "Bank: 0x10000\n");
                        fprintf(stderr, "Enter the ID(hex): ");
                        scndata("%x", &ID);
                        fprintf(stderr, "Enter the mask(hex): ");
                        scndata("%x", &mask);
                        fprintf(stderr, "Enter the Direction(hex): ");
                        scndata("%x", &value);
                        EapiStatus = EApiGPIOSetDirection(ID, mask, value);
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Set GPIO Direction not
support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Set GPIO Direction successful\n\n");
                        }
                        break;
                case 4:
                        fprintf(stderr, "Bank: 0x10000\n");
                        fprintf(stderr, "Enter the ID(hex): ");
                        scndata("%x", &ID);
                        fprintf(stderr, "Enter the mask(hex): ");
                        scndata("%x", &mask);
                        EapiStatus = EApiGPIOGetLevel(ID, mask, &value);
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Get GPIO Level not support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Get GPIO Level ID: %x, mask: %x,
Level: %x\n\n", ID, mask, value);
                        }
                        break;
                case 5:
                        fprintf(stderr, "Bank: 0x10000\n");
                        fprintf(stderr, "Enter the ID(hex): ");
                        scndata("%x", &ID);
                        fprintf(stderr, "Enter the mask(hex): ");
                        scndata("%x", &mask);
                        fprintf(stderr, "Enter the Level(hex): ");
                        scndata("%x", &value);
                        EapiStatus = EApiGPIOSetLevel(ID, mask, value);
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Set GPIO Level not support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Set GPIO Level successful\n\n");
                        }
                        break;
                        break;
                case 6:
                        fprintf(stderr, "Exit program!!!\n\n");
```

```
                                        break;
                                default:
                                        fprintf(stderr, "GPIO error!!!\n\n");
                                        break;
                                }
                                fprintf(stderr, "*****************************************\n");
                }

}


// ****************************************
// Main
// ****************************************
int main()
{
        int select = 0;




        if (InitLibrary() != 0)
        {
                                fprintf(stderr,"---- intialize: fail\n");

            // system("pause");
              return 1;
        }
                fprintf(stderr, "---- intialize: ok\n");



                        GPIO_demo();


       // system("pause");
        return 0;
}
```