



**MODEL:**  
**tKINO-ULT3**

**Thin Mini-ITX SBC with 14nm Intel® Core™ i7/i5/i3 or Celeron®  
On-board SoC, Dual HDMI, LVDS/eDP, Dual GbE, USB 3.0, PCIe Mini,  
SATA 6Gb/s, eMMC 5.0, RS-232/422/485, HD Audio, and RoHS**

# User Manual

# Revision

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| Date             | Version | Changes                                     |
|------------------|---------|---|
| October 11, 2017 | 1.01    | Modified <i>Section 2.4: Optional Items</i> |
| March 30, 2017   | 1.00    | Initial release                             |

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# Manual Conventions

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## **WARNING**

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.



## **CAUTION**

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.



## **NOTE**

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.



## **HOT SURFACE**

This symbol indicates a hot surface that should not be touched without taking care.

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Chapter

1

# Introduction

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## 1.1 Introduction



**Figure 1-1: tKINO-ULT3**

The tKINO-ULT3 series is a Mini-ITX form factor single board computer. It has an on-board 14nm Intel® Core™ i7/i5/i3 or Celeron® processor, and supports two 260-pin 2133 MHz dual-channel DDR4 SDRAM SO-DIMM slots with up to 32.0 GB of memory.

The tKINO-ULT3 series includes an internal LVDS/eDP connector, one HDMI connector and one HDMI/DP combo connector for triple independent display.

Expansion and I/O include two full-size PCIe Mini slots supporting mSATA and 3G modules, four USB 3.0 connectors on the rear panel, four USB 2.0 connectors by pin header and two SATA 6Gb/s connectors. Serial device connectivity is provided by four internal RS-232 connectors and two internal RS-232/422/485 connectors. Two RJ-45 GbE connectors provide the system with smooth connections to an external LAN. One on-board SIM card socket also supports for 3G/LTE expansion.



## 1.2 Model Variations

The model variations of the tKINO-ULT3 series are listed below.

| Model No.         | SoC  |
|-------------------|--|
| tKINO-ULT3-i7-R10 | Intel® Core™ i7-6600U on-board SoC<br>(up to 3.4 GHz, dual-core, 4 MB cache, TDP=15 W) |
| tKINO-ULT3-i5-R10 | Intel® Core™ i5-6300U on-board SoC<br>(up to 3.0 GHz, dual-core, 3 MB cache, TDP=15 W) |
| tKINO-ULT3-i3-R10 | Intel® Core™ i3-6100U on-board SoC<br>(up to 2.3 GHz, dual-core, 3 MB cache, TDP=15 W) |
| tKINO-ULT3-C-R10  | Intel® Celeron® 3955U on-board SoC<br>(up to 2.0 GHz, dual-core, 2 MB cache, TDP=15 W) |
| tKINO-ULT3-CE-R10 | Intel® Celeron® 3855U on-board SoC<br>(up to 1.6 GHz, dual-core, 2 MB cache, TDP=15 W) |

**Table 1-1: tKINO-ULT3 Model Variations**

## 1.3 Features

Some of the tKINO-ULT3 motherboard features are listed below:

- Thin Mini-ITX motherboard with 6<sup>th</sup> generation Intel® ULT processor
- Triple independent display
- Two 2133 MHz DDR4 SO-DIMM slots support up to 32 GB of memory
- Easy assembly heatsink module (with or without fan) for thermal management
- One full-size PCIe Mini card slot with SIM card socket for 3G/LTE expansion
- One full-size PCIe Mini card slot supports mSATA modules
- Two SATA 6Gb/s connectors with power output
- Four USB 3.0 external connectors
- Four RS-232 connectors and two RS-232/422/485 connectors
- Optional eMMC 5.0 up to 32 GB
- IEI One Key Recovery solution allows you to create rapid OS backup and recovery

## 1.4 Connectors

The connectors on the tKINO-ULT3 are shown in the figure below.

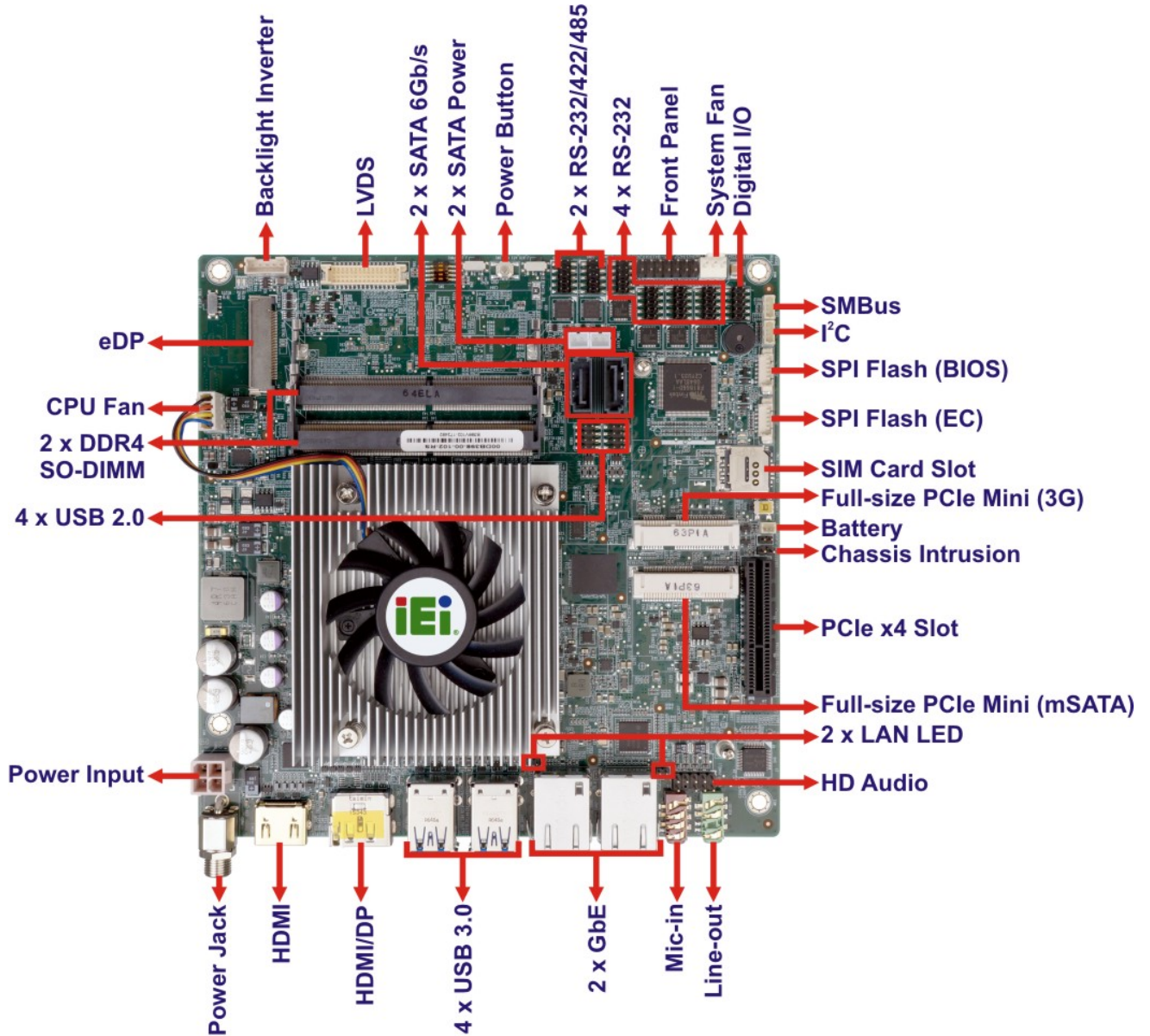


Figure 1-2: Connectors (Front Side)

tKINO-ULT3 SBC

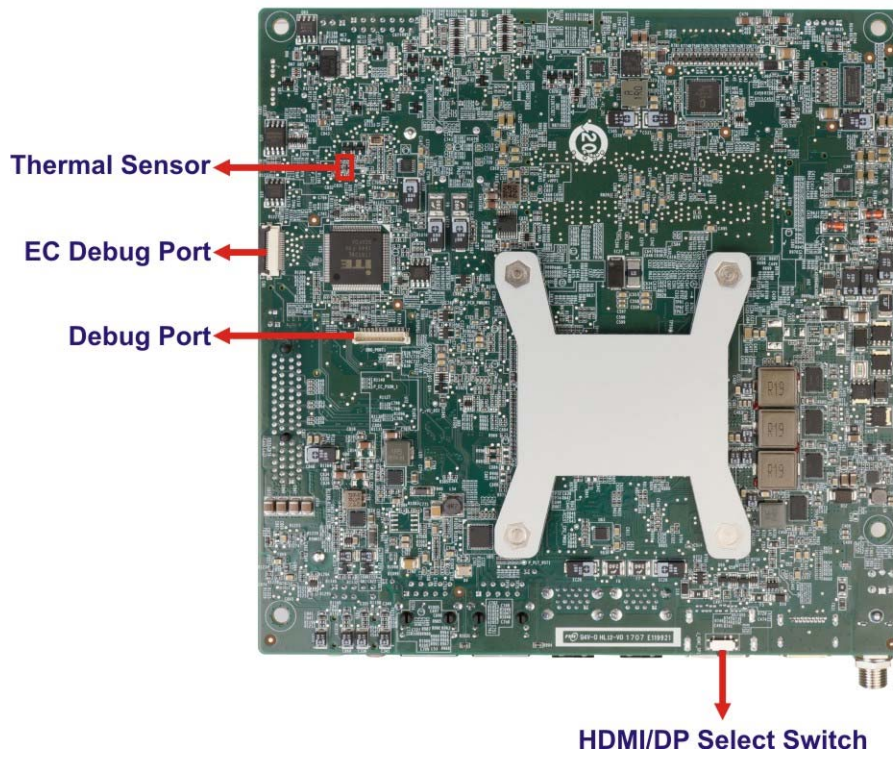


Figure 1-3: Connectors (Solder Side)

## 1.5 Dimensions

Figure 1-4 shows the dimensions of the tKINO-ULT3 installed with the standard heatsink (with fan).

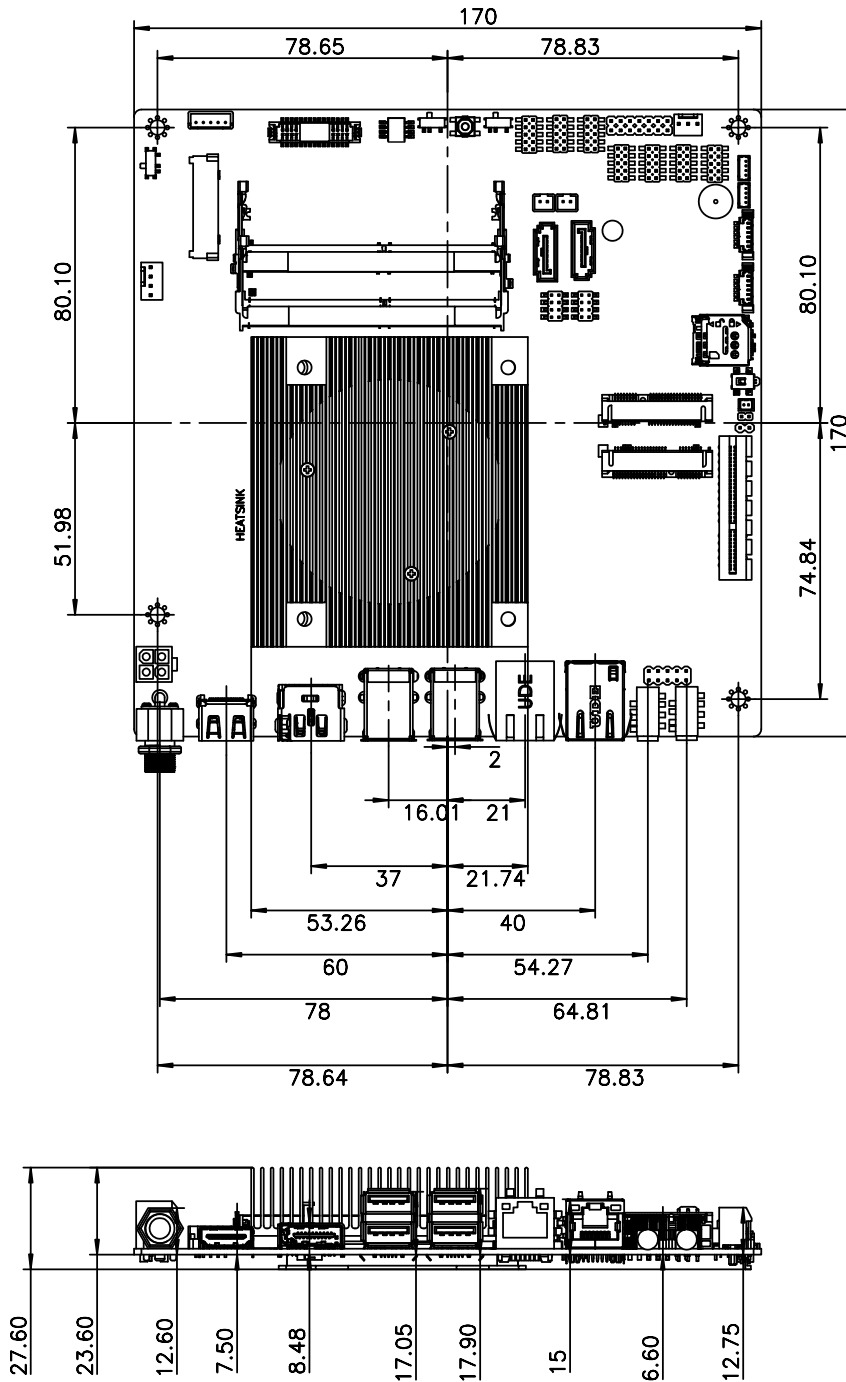


Figure 1-4: Dimensions with Standard Heatsink (mm)

tKINO-ULT3 SBC

Figure 1-5 shows the dimensions of the tKINO-ULT3 installed with the optional heatsink (without fan, P/N: 34000-000645-RS).

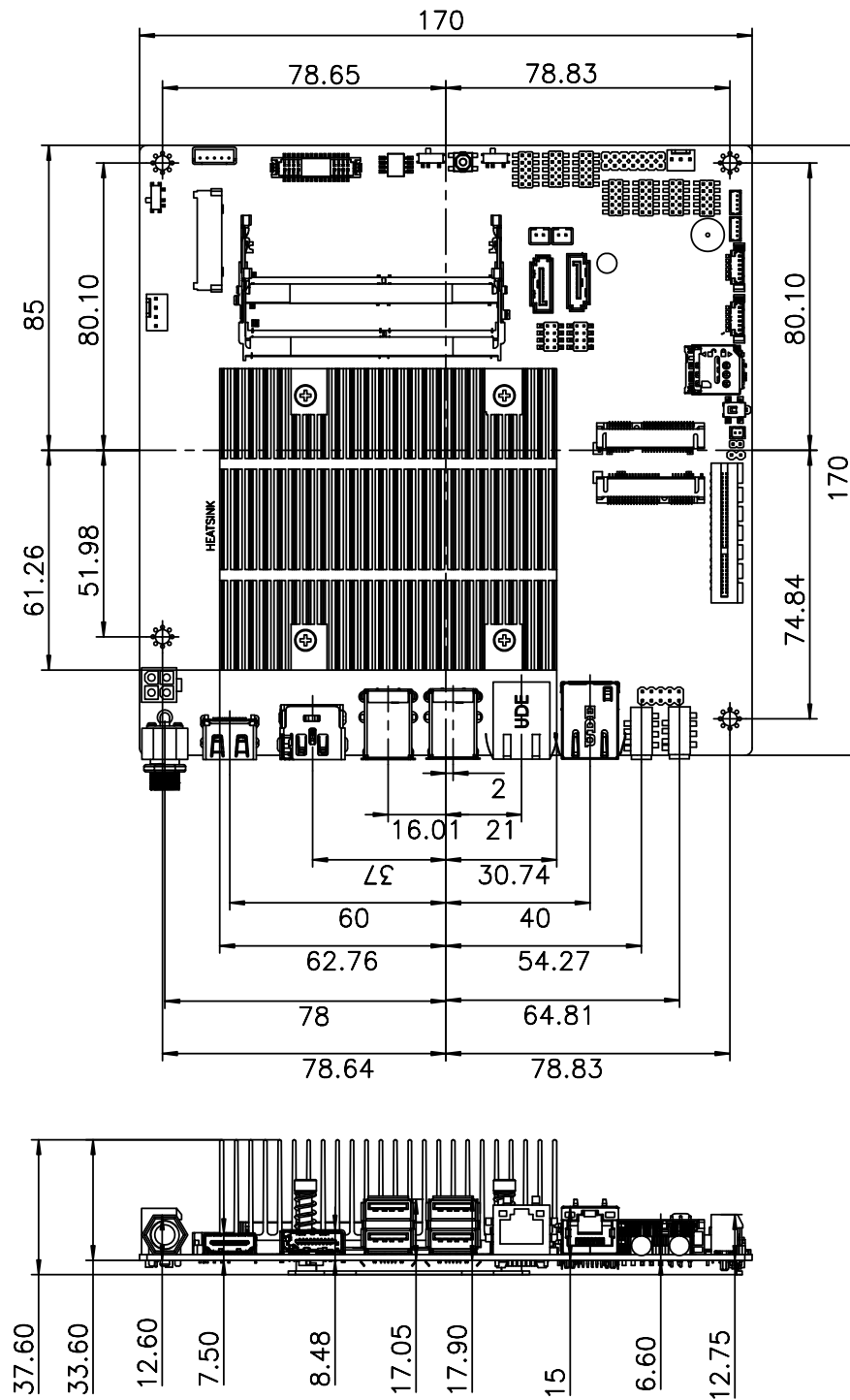


Figure 1-5: Dimensions with Optional Heatsink (mm)

## 1.6 Data Flow

Figure 1-6 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

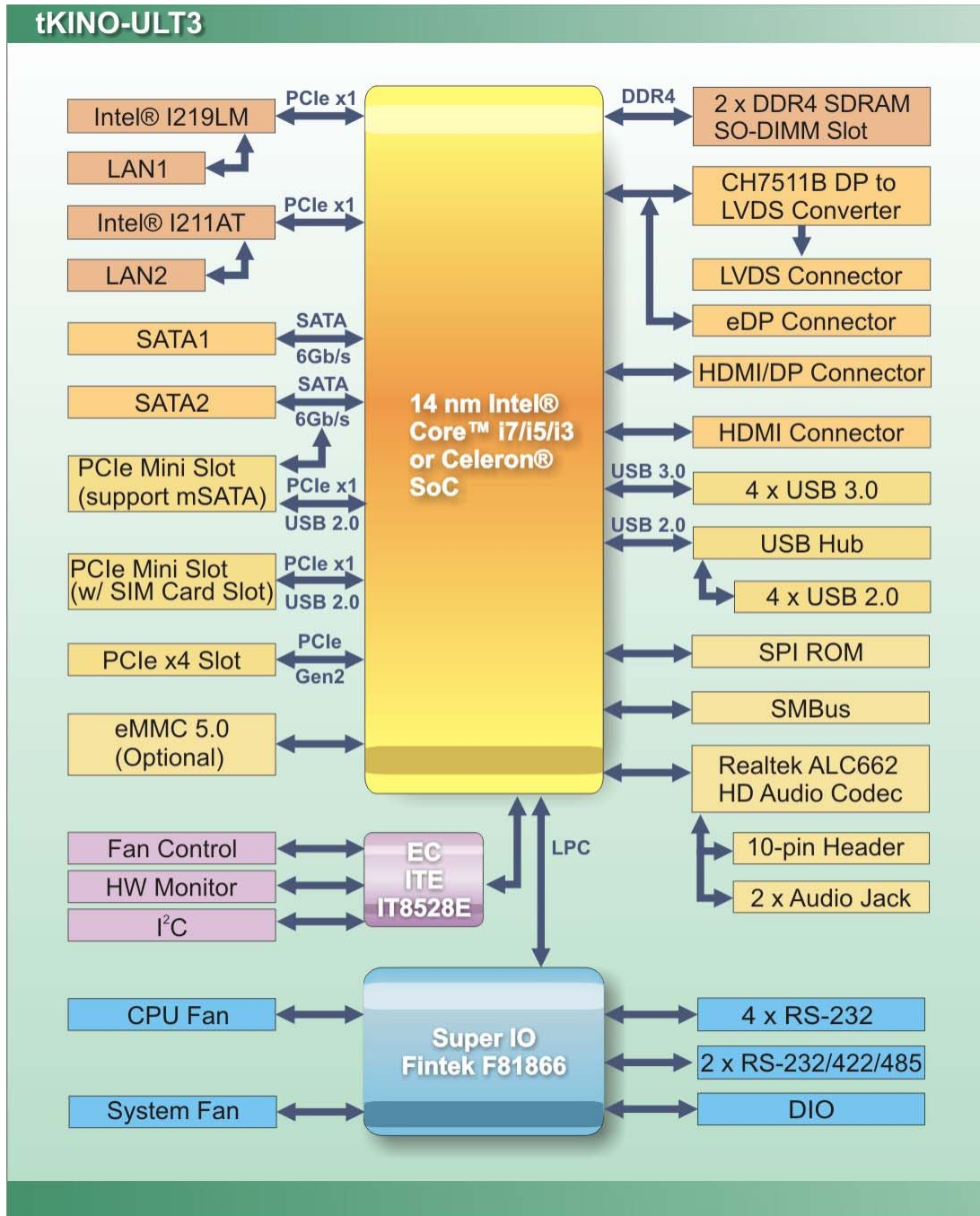


Figure 1-6: Data Flow Diagram

## tKINO-ULT3 SBC

### 1.7 Technical Specifications

tKINO-ULT3 technical specifications are listed below.

| Specification              | tKINO-ULT3   |
|----------------------------|--|
| <b>SoC</b>                 | 6 <sup>th</sup> generation Intel® mobile ULT on-board SoC: <ul style="list-style-type: none"> <li>▪ Intel® Core™ i7-6600U on-board SoC<br/>(up to 3.4 GHz, dual-core, 4 MB cache, TDP=15 W)</li> <li>▪ Intel® Core™ i5-6300U on-board SoC<br/>(up to 3.0 GHz, dual-core, 3 MB cache, TDP=15 W)</li> <li>▪ Intel® Core™ i3-6100U on-board SoC<br/>(up to 2.3 GHz, dual-core, 3 MB cache, TDP=15 W)</li> <li>▪ Intel® Celeron® 3955U on-board SoC<br/>(up to 2.0 GHz, dual-core, 2 MB cache, TDP=15 W)</li> <li>▪ Intel® Celeron® 3855U on-board SoC<br/>(up to 1.6 GHz, dual-core, 2 MB cache, TDP=15 W)</li> </ul> |
| <b>BIOS</b>                | AMI UEFI BIOS  |
| <b>Memory</b>              | Two 260-pin 2133 MHz dual-channel DDR4 SO-DIMM slots<br>(system max. 32 GB)  |
| <b>Graphics</b>            | 9 <sup>th</sup> generation Intel® HD Graphics  |
| <b>Display Output</b>      | Triple independent display<br>1 x HDMI 2.4 (up to 4096x2160 @ 24 Hz)<br>1 x HDMI/DP (up to 4096x2160 @ 24 Hz)<br>1 x LVDS/eDP (selected by switch)   |
| <b>Ethernet</b>            | LAN1: Intel® I219-LM PHY with Intel® AMT 11.0 support<br>LAN2: Intel® I211-AT PCIe GbE controller with NCSI support  |
| <b>Digital I/O</b>         | 8-bit digital I/O by 10-pin (2x5) header   |
| <b>Super IO</b>            | Fintek F81866D-I   |
| <b>Embedded Controller</b> | ITE IT8528E/FX   |
| <b>Audio</b>               | Realtek ALC662 HD codec  |
| <b>Watchdog Timer</b>      | Software programmable support 1~255 sec. system reset  |

| Specification                                 | tKINO-ULT3  |
|---|---|
| <b>I/O Interface</b>                          |   |
| <b>Audio Connector</b>                        | 2 x Audio jack (line-out, mic-in) on rear I/O<br>1 x Analog audio by 10-pin (2x5) header  |
| <b>Ethernet</b>                               | 2 x RJ-45 GbE port  |
| <b>Serial Ports</b>                           | 2 x RS-232/422/485 by 10-pin (2x5) header<br>4 x RS-232 by 10-pin (2x5) header  |
| <b>USB Ports</b>                              | 4 x USB 3.0 on rear I/O<br>4 x USB 2.0 by 8-pin (2x4) header  |
| <b>Front Panel</b>                            | 1 x Front panel connector by 14-pin (2x7) header (for connecting power LED, HDD LED, power button and reset button)   |
| <b>LAN LED</b>                                | 2 x LAN link LED connector by 2-pin header  |
| <b>Fan</b>                                    | 1 x CPU fan connector by 4-pin (1x4) wafer<br>1 x System fan connector by 3-pin (1x3) wafer   |
| <b>SMBus</b>                                  | 1 x SMBus connector by 4-pin (1x4) wafer  |
| <b>I<sup>2</sup>C</b>                         | 1 x I <sup>2</sup> C connector by 4-pin (1x4) wafer   |
| <b>Storage</b>                                | 2 x SATA 6Gb/s with 5 V SATA power connectors<br>Optional eMMC 5.0 (up to 32 GB)  |
| <b>Expansion</b>                              | 1 x PCIe x4 slot<br>1 x Full-size PCIe Mini card slot (support mSATA, colay SATA2)<br>1 x Full-size PCIe Mini card slot (with SIM card socket)<br><i>*3855U CPU belongs to Skylake ULT Base series which supports PCIe Gen 2 signal only.</i> |
| <b>Environmental and Power Specifications</b> |   |
| <b>Power Supply</b>                           | 9 V ~ 36 V DC input (AT/ATX power mode)   |
| <b>Power Connector</b>                        | 1 x Internal power connector by 4-pin (2x2) connector<br>1 x External DC power jack (Ø5.5mm)  |
| <b>Power Consumption</b>                      | 12 V @ 4.68 A (Intel® Core™ i7-6600U up to 3.4 GHz CPU with 16 GB (two 8 GB) DDR4 2133 MHz memory running in 3.2 GHz)   |



## tKINO-ULT3 SBC

| Specification                  | tKINO-ULT3               |
|--------------------------------|--------------------------|
| Operating Temperature          | -20°C ~ 60°C             |
| Storage Temperature            | -30°C ~ 70°C             |
| Humidity                       | 5% ~ 95%, non-condensing |
| <b>Physical Specifications</b> |                          |
| Dimensions                     | 170 mm x 170 mm          |
| Weight GW/NW                   | 900 g / 375 g            |

**Table 1-2: Technical Specifications**

Chapter

**2**

# Unpacking

---

## 2.1 Anti-static Precautions

---



### WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

---

Make sure to adhere to the following guidelines:

- **Wear an anti-static wristband:** Wearing an anti-static wristband can prevent electrostatic discharge.
- **Self-grounding:** Touch a grounded conductor every few minutes to discharge any excess static buildup.
- **Use an anti-static pad:** When configuring any circuit board, place it on an anti-static mat.
- **Only handle the edges of the PCB:** Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

## 2.2 Unpacking Precautions

When the tKINO-ULT3 is unpacked, please do the following:

- Follow the antistatic guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.






## 2.3 Packing List




**NOTE:**

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the tKINO-ULT3 was purchased from or contact an IEI sales representative directly by sending an email to [sales@ieiworld.com](mailto:sales@ieiworld.com).

The tKINO-ULT3 is shipped with the following components:



| Quantity | Item and Part Number             | Image   |
|----------|----------------------------------|---|
| 1        | tKINO-ULT3 single board computer |   |
| 2        | SATA with power cable kit        |  |
| 1        | I/O shielding                    |  |
| 1        | Utility CD                       |  |
| 1        | One Key Recovery CD              |  |

**tKINO-ULT3 SBC**

|   |                          |   |
|---|--------------------------|---|
| 1 | Quick Installation Guide |  |
|---|--------------------------|---|

**2.4 Optional Items**

The following are optional components which may be separately purchased:

| Item and Part Number   | Image  |
|--|--|
| RS-232 cable, 200 mm, p=2.0 mm<br>(P/N: 32205-002700-100-RS)               |   |
| Fanless heatsink module, 93.5 mm x 84 mm x 30 mm<br>(P/N: 34000-000645-RS) |  |

Chapter

**3**

# Connectors

---

## tKINO-ULT3 SBC

### 3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

#### 3.1.1 tKINO-ULT3 Layout

The figures below show all the connectors and jumpers.

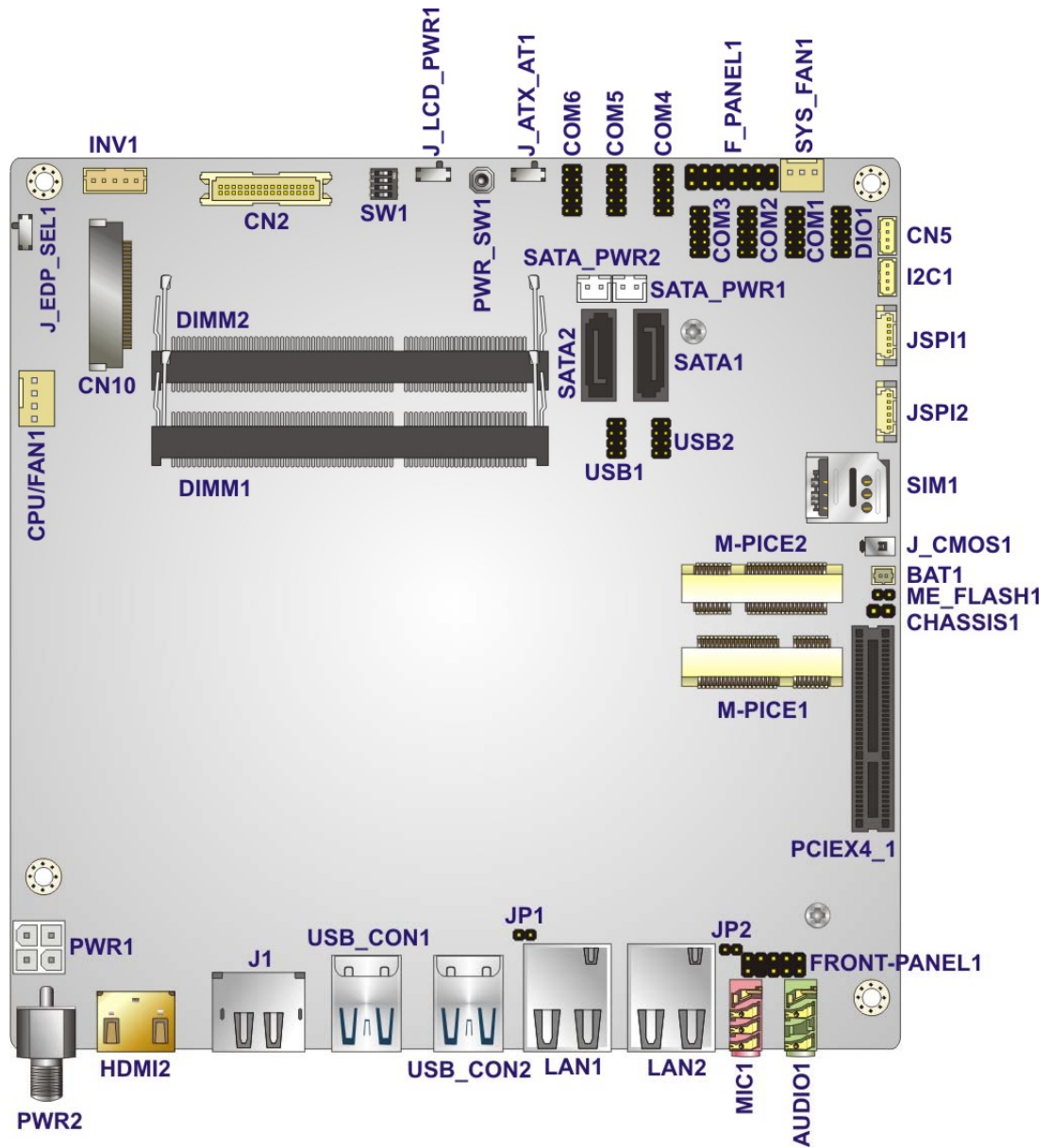


Figure 3-1: Connector and Jumper Locations

### 3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

| Connector                              | Type                     | Label                     |
|--|--------------------------|---------------------------|
| Audio connector                        | 10-pin header            | FRONT-PANEL1              |
| Battery connector                      | 2-pin wafer              | BAT1                      |
| Chassis intrusion connector            | 2-pin header             | CHASSIS1                  |
| DC-IN power connector                  | 4-pin Molex              | PWR1                      |
| Digital I/O connector                  | 10-pin header            | DIO1                      |
| eDP connector                          | 40-pin connector         | CN10                      |
| Fan connector, CPU                     | 4-pin wafer              | CPU/FAN1                  |
| Fan connector, system                  | 3-pin wafer              | SYS_FAN1                  |
| Front panel connector                  | 14-pin header            | F_PANEL1                  |
| I <sup>2</sup> C connector             | 4-pin wafer              | I2C1                      |
| LCD backlight inverter connector       | 5-pin wafer              | INV1                      |
| LVDS LCD connector                     | 30-pin crimp             | CN2                       |
| LAN LED connectors                     | 2-pin header             | JP1, JP2                  |
| Memory slots                           | 260-pin DDR4 SO-DIMM     | DIMM1, DIMM2              |
| PCIe x4 slot                           | PCIe x4 slot             | PCIEX4_1                  |
| PCIe Mini card slot (for mSATA module) | Full-size PCIe Mini slot | M_PICE1                   |
| PCIe Mini card slot (for 3G module)    | Full-size PCIe Mini slot | M_PICE2                   |
| Power button (on board)                | Push button              | PWR_SW1                   |
| RS-232 serial port connectors          | 10-pin header            | COM1, COM2,<br>COM3, COM4 |
| RS-232/422/485 serial port connectors  | 10-pin header            | COM5, COM6                |



## tKINO-ULT3 SBC

|                             |                      |                         |
|-----------------------------|----------------------|-------------------------|
| SATA 6Gb/s drive connectors | 7-pin SATA connector | SATA1, SATA2            |
| SATA power connectors       | 2-pin wafer          | SATA_PWR1,<br>SATA_PWR2 |
| SMBus connector             | 4-pin wafer          | CN5                     |
| SIM card slot               | SIM slot             | SIM1                    |
| SPI flash connector, BIOS   | 6-pin wafer          | JSPI1                   |
| SPI flash connector, EC     | 6-pin wafer          | JSPI2                   |
| USB 2.0 connectors          | 8-pin header         | USB1, USB2              |

**Table 3-1: Peripheral Interface Connectors**

### 3.1.3 External Interface Panel Connectors

The table below lists the connectors on the external I/O panel.

| Connector               | Type       | Label                 |
|-------------------------|------------|-----------------------|
| Audio line-out jack     | Audio jack | AUDIO1                |
| Audio mic-in jack       | Audio jack | MIC1                  |
| HDMI connector          | HDMI       | HDMI2                 |
| HDMI/DP combo connector | HDMI+DP    | J1                    |
| LAN connectors          | RJ-45      | LAN1, LAN2            |
| Power input connector   | Power jack | PWR2                  |
| USB 3.0 connectors      | USB 3.0    | USB_CON1,<br>USB_CON2 |

**Table 3-2: Rear Panel Connectors**

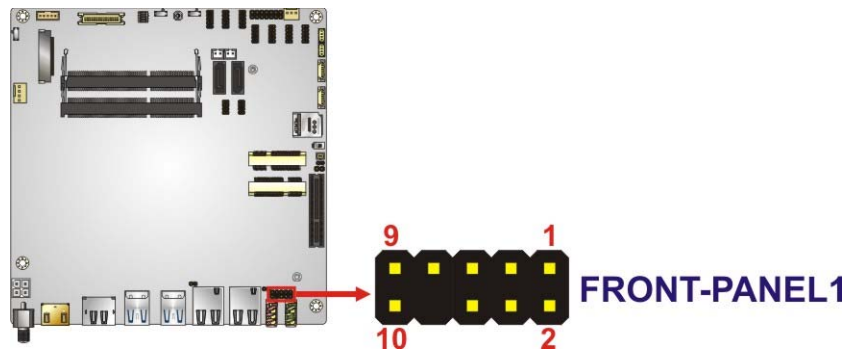
### 3.2 Internal Peripheral Connectors

The section describes all of the connectors on the tKINO-ULT3.

#### 3.2.1 Audio Connector

- CN Label:** FRONT-PANEL1
- CN Type:** 10-pin header, p=2.54 mm
- CN Location:** See **Figure 3-2**
- CN Pinouts:** See **Table 3-3**

The audio connector is connected to external audio devices including speakers and microphones for the input and output of audio signals to and from the system.



**Figure 3-2: Audio Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1       | MIC2-L      | 2       | GND         |
| 3       | MIC2-R      | 4       | Presence#   |
| 5       | LINE2-R     | 6       | MIC2-JD     |
| 7       | FRONT-IO    | 8       | NC          |
| 9       | LINE2-L     | 10      | LINE2-JD    |

**Table 3-3: Audio Connector Pinouts**

tKINO-ULT3 SBC

3.2.2 Battery Connector



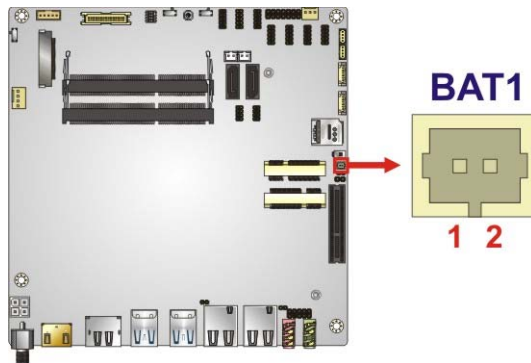
**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- CN Label:**            **BAT1**
- CN Type:**            2-pin wafer, p=1.25 mm
- CN Location:**        See **Figure 3-3**
- CN Pinouts:**         See **Table 3-4**

The battery connector is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off.



**Figure 3-3: Battery Connector Location**

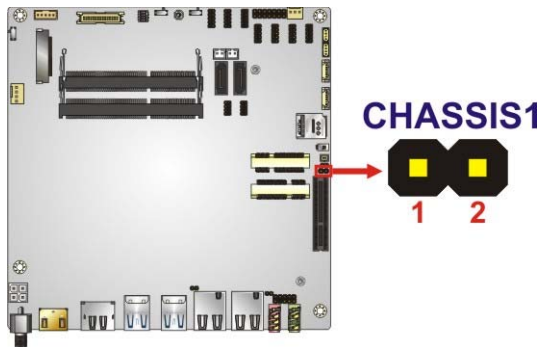
| Pin | Description |
|-----|-------------|
| 1   | VBAT+       |
| 2   | GND         |

**Table 3-4: Battery Connector Pinouts**

### 3.2.3 Chassis Intrusion Connector

- CN Label:** CHASSIS1
- CN Type:** 2-pin header, p=2.54 mm
- CN Location:** See **Figure 3-4**
- CN Pinouts:** See **Table 3-5**

The chassis intrusion connector is for a chassis intrusion detection sensor or switch that detects if a chassis component is removed or replaced.



**Figure 3-4: Chassis Intrusion Connector Location**

| Pin | Description |
|-----|-------------|
| 1   | -CASEOPEN   |
| 2   | GND         |

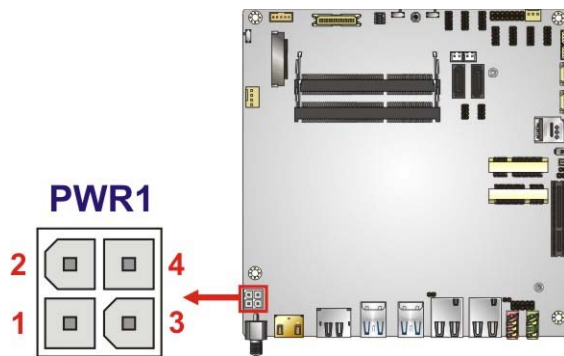
**Table 3-5: Chassis Intrusion Connector Pinouts**

**tKINO-ULT3 SBC**

**3.2.4 DC-IN Power Connector**

- CN Label:** PWR1
- CN Type:** 4-pin Molex, p=4.2 mm
- CN Location:** See **Figure 3-5**
- CN Pinouts:** See **Table 3-6**

The connector supports 9 V ~ 36 V power supply.



**Figure 3-5: DC-IN Power Connector Location**

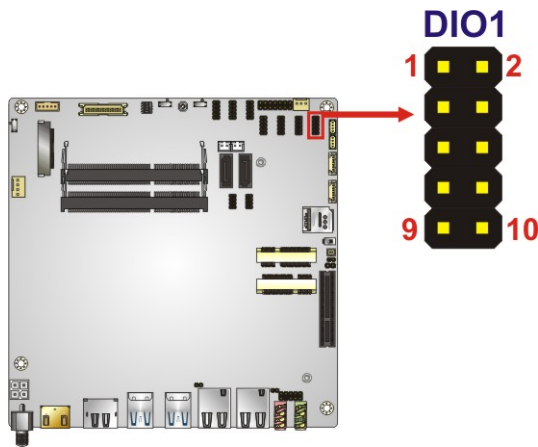
| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1       | GND         | 2       | GND         |
| 3       | PWR         | 4       | PWR         |

**Table 3-6: DC-IN Power Connector Pinouts**

### 3.2.5 Digital I/O Connector

- CN Label:** DIO1
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-6**
- CN Pinouts:** See **Table 3-7**

The 8-bit digital I/O connector provides programmable input and output for external devices.



**Figure 3-6: Digital I/O Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1       | GND         | 2       | VCC         |
| 3       | Output 3    | 4       | Output 2    |
| 5       | Output 1    | 6       | Output 0    |
| 7       | Input 3     | 8       | Input 2     |
| 9       | Input 1     | 10      | Input 0     |

**Table 3-7: Digital I/O Connector Pinouts**

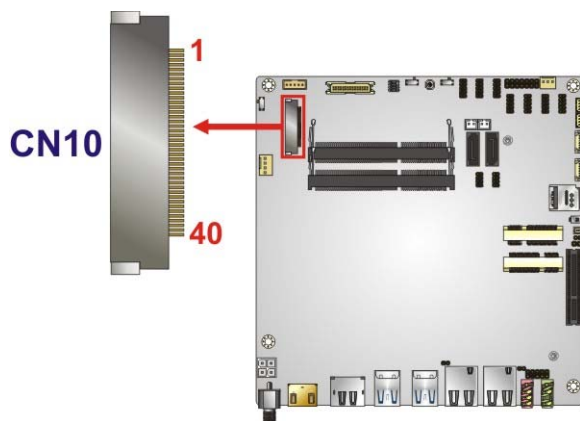
### 3.2.6 eDP Connector

**NOTE:**

The eDP connector is disabled by default since the eDP connector is co-lay with the LVDS connector. To enable the eDP connector, use the LVDS/eDP select switch to configure the settings. Please refer to **Section 4.6.5** for detailed information.

|                     |                             |
|---------------------|-----------------------------|
| <b>CN Label:</b>    | <b>CN10</b>                 |
| <b>CN Type:</b>     | 40-pin connector, p=0.50 mm |
| <b>CN Location:</b> | See <b>Figure 3-7</b>       |
| <b>CN Pinouts:</b>  | See <b>Table 3-8</b>        |

The eDP connector supports various high-performance display devices.



**Figure 3-7: eDP Connector Location**

| Pin | Description         | Pin | Description         |
|-----|---------------------|-----|---------------------|
| 1   | NC                  | 21  | VCC_LCD (3.3V only) |
| 2   | GND                 | 22  | NC                  |
| 3   | (eDP_TX3-)          | 23  | GND                 |
| 4   | (eDP_TX3+)          | 24  | GND                 |
| 5   | GND                 | 25  | GND                 |
| 6   | (eDP_TX2-)          | 26  | GND                 |
| 7   | (eDP_TX2+)          | 27  | eDP_HPD             |
| 8   | GND                 | 28  | GND                 |
| 9   | (eDP_TX1-)          | 29  | GND                 |
| 10  | (eDP_TX1+)          | 30  | GND                 |
| 11  | GND                 | 31  | GND                 |
| 12  | (eDP_TX0-)          | 32  | (eDP_BKLT_EN)       |
| 13  | (eDP_TX0+)          | 33  | (eDP_BKLT_CRTL)     |
| 14  | GND                 | 34  | NC                  |
| 15  | (eDP_AUX+)          | 35  | NC                  |
| 16  | (eDP_AUX-)          | 36  | BKLT_PWR            |
| 17  | GND                 | 37  | BKLT_PWR            |
| 18  | VCC_LCD (3.3V only) | 38  | BKLT_PWR            |
| 19  | VCC_LCD (3.3V only) | 39  | BKLT_PWR            |
| 20  | VCC_LCD (3.3V only) | 40  | NC                  |

**Table 3-8: eDP Connector Pinouts**



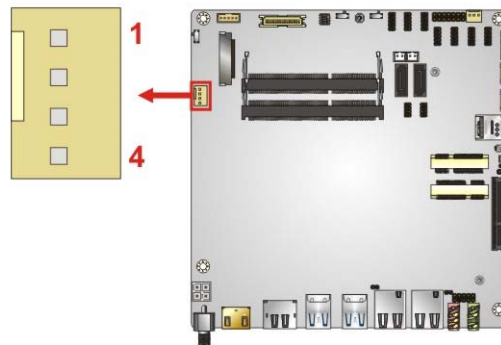
**tKINO-ULT3 SBC**

**3.2.7 Fan Connector, CPU**

- CN Label:** CPU/FAN1
- CN Type:** 4-pin wafer, p=2.54 mm
- CN Location:** See **Figure 3-8**
- CN Pinouts:** See **Table 3-9**

The CPU fan connector attaches to a CPU cooling fan.

**CPU/FAN1**



**Figure 3-8: CPU Fan Connector Location**

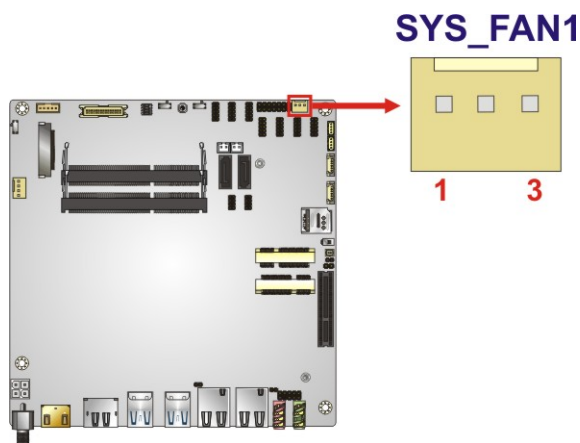
| Pin | Description |
|-----|-------------|
| 1   | GND         |
| 2   | +12V        |
| 3   | FANIO       |
| 4   | PWM         |

**Table 3-9: CPU Fan Connector Pinouts**

### 3.2.8 Fan Connector, System

- CN Label:**        **SYS\_FAN1**
- CN Type:**        3-pin wafer, p=2.54 mm
- CN Location:**    See **Figure 3-9**
- CN Pinouts:**     See **Table 3-10**

The system fan connector attaches to a system cooling fan.



**Figure 3-9: System Fan Connector Location**

| Pin | Description |
|-----|-------------|
| 1   | FANIO       |
| 2   | +12V (PWM)  |
| 3   | GND         |

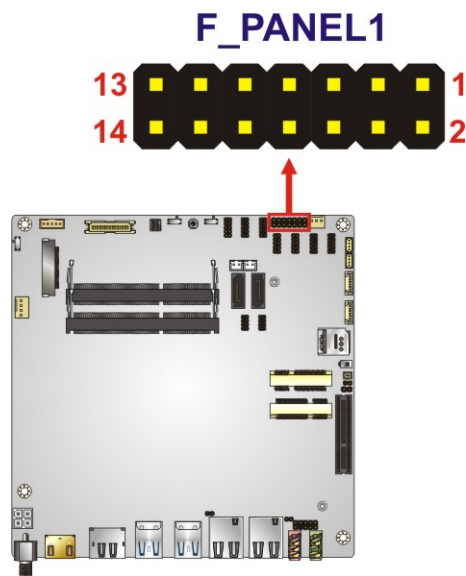
**Table 3-10: System Fan Connector Pinouts**

## tKINO-ULT3 SBC

### 3.2.9 Front Panel Connector

- CN Label:** F\_PANEL1
- CN Type:** 14-pin wafer, p=2.54 mm
- CN Location:** See **Figure 3-10**
- CN Pinouts:** See **Table 3-11**

The front panel connector connects to the power button, reset button, speaker, IPMI LED indicator, power LED indicator and HDD LED indicator on the system front panel.



**Figure 3-10: Front Panel Connector Location**

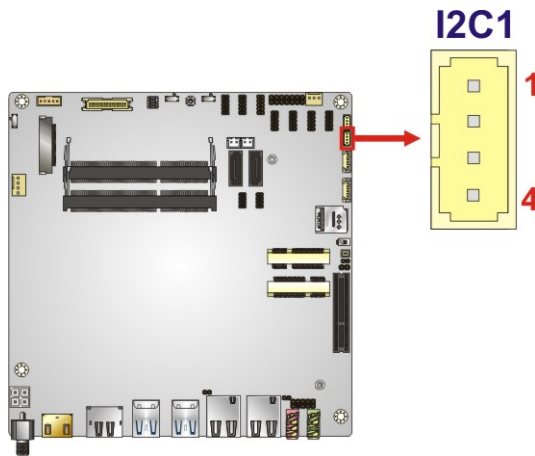
| Function     | Pin | Description | Function     | Pin | Description  |
|--------------|-----|-------------|--------------|-----|--------------|
| Power LED    | 1   | +5V         | Speaker      | 2   | BEEP_PWR     |
|              | 3   | NC          | IPMI LED     | 4   | IPMI ID_LED+ |
|              | 5   | GND         |              | 6   | IPMI ID_LED- |
| Power Button | 7   | PWRBTN_SW#  | Speaker      | 8   | PC_BEEP      |
|              | 9   | GND         |              | 10  | NC           |
| HDD LED      | 11  | +5V         | Reset Button | 12  | EXTRST-      |
|              | 13  | SATA_LED#   |              | 14  | GND          |

**Table 3-11: Front Panel Connector Pinouts**

### 3.2.10 I<sup>2</sup>C Connector

- CN Label:** I2C1
- CN Type:** 4-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-11**
- CN Pinouts:** See **Table 3-12**

The I<sup>2</sup>C connector is used to connect I<sup>2</sup>C-bus devices to the motherboard.



**Figure 3-11: I<sup>2</sup>C Connector Location**

| Pin | Description |
|-----|-------------|
| 1   | GND         |
| 2   | I2C_DATA    |
| 3   | I2C_CLK     |
| 4   | +5V         |

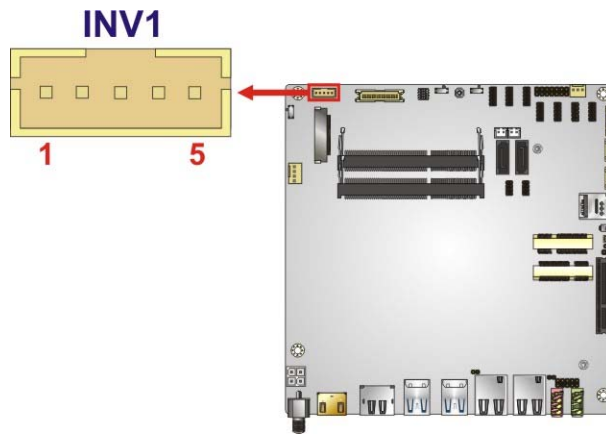
**Table 3-12: I<sup>2</sup>C Connector Pinouts**

**tKINO-ULT3 SBC**

**3.2.11 LVDS Backlight Inverter Connector**

- CN Label:** INV1
- CN Type:** 5-pin wafer, p=2.00 mm
- CN Location:** See **Figure 3-12**
- CN Pinouts:** See **Table 3-13**

The backlight inverter connector provides power to an LCD panel.



**Figure 3-12: Backlight Inverter Connector Location**

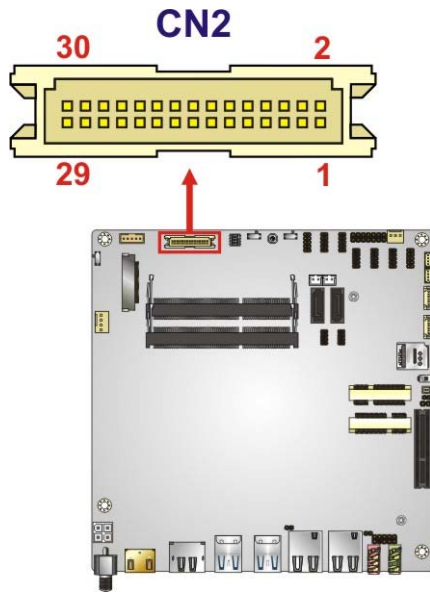
| Pin | Description      |
|-----|------------------|
| 1   | LCD_BKLTCTL      |
| 2   | GND              |
| 3   | +12V             |
| 4   | GND              |
| 5   | BACKLIGHT_ENABLE |

**Table 3-13: Backlight Inverter Connector Pinouts**

### 3.2.12 LVDS LCD Connector

- CN Label:** CN2
- CN Type:** 30-pin crimp, p=1.25 mm
- CN Location:** See **Figure 3-13**
- CN Pinouts:** See **Table 3-14**

The LVDS connector is for an LCD panel to connect to the board.



**Figure 3-13: LVDS Connector Location**

| Pin | Description    | Pin | Description    |
|-----|----------------|-----|----------------|
| 1   | GROUND         | 2   | GROUND         |
| 3   | LVDS_A_TX0-P   | 4   | LVDS_A_TX0-N   |
| 5   | LVDS_A_TX1-P   | 6   | LVDS_A_TX1-N   |
| 7   | LVDS_A_TX2-P   | 8   | LVDS_A_TX2-N   |
| 9   | LVDS_A_TXCLK-P | 10  | LVDS_A_TXCLK-N |
| 11  | LVDS_A_TX3-P   | 12  | LVDS_A_TX3-N   |
| 13  | GROUND         | 14  | GROUND         |
| 15  | LVDS_B_TX0-P   | 16  | LVDS_B_TX0-N   |
| 17  | LVDS_B_TX1-P   | 18  | LVDS_B_TX1-N   |
| 19  | LVDS_B_TX2-P   | 20  | LVDS_B_TX2-N   |

tKINO-ULT3 SBC

| Pin | Description    | Pin | Description    |
|-----|----------------|-----|----------------|
| 21  | LVDS_B_TXCLK-P | 22  | LVDS_B_TXCLK-N |
| 23  | LVDS_B_TX3-P   | 24  | LVDS_B_TX3-N   |
| 25  | GROUND         | 26  | GROUND         |
| 27  | +LCD VCC       | 28  | +LCD VCC       |
| 29  | +LCD VCC       | 30  | +LCD VCC       |

Table 3-14: LVDS Connector Pinouts

3.2.13 LAN LED Connectors

- CN Label:** JP1, JP2
- CN Type:** 2-pin header, p=2.00 mm
- CN Location:** See Figure 3-14
- CN Pinouts:** See Table 3-15

The LAN LED connectors connect to the LAN link LEDs on the system.

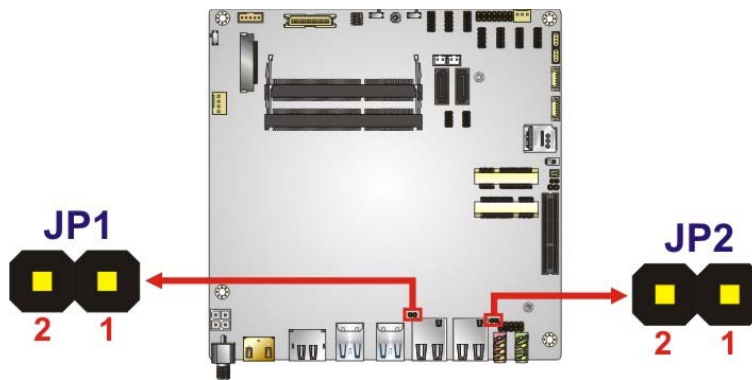


Figure 3-14: LAN LED Connector Locations

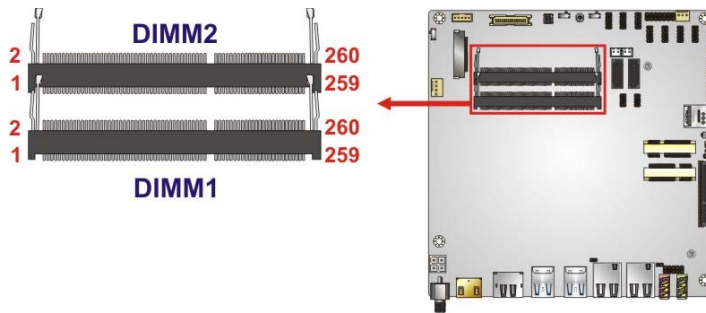
| Pin | Description       |
|-----|-------------------|
| 1   | +3.3VLAN          |
| 2   | LAN_LED_LINK#_ACT |

Table 3-15: LAN LED Connector Pinouts

### 3.2.14 Memory Slot

- CN Label:** DIMM1, DIMM2
- CN Type:** 260-pin DDR4 SO-DIMM slot
- CN Location:** See **Figure 3-15**

The memory slots accept DDR4 SO-DIMM.

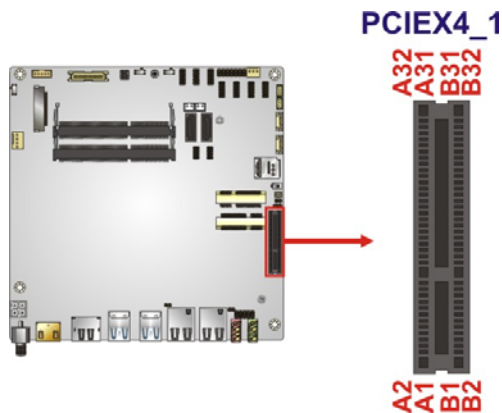


**Figure 3-15: Memory Slot Locations**

### 3.2.15 PCI Express x4 Slot

- CN Label:** PCIEX4\_1
- CN Type:** PCIe x4 slot
- CN Location:** See **Figure 3-16**

The PCIe x4 expansion card slot is for PCIe x4 expansion cards.



**Figure 3-16: PCIe x4 Slot Location**



tKINO-ULT3 SBC

3.2.16 PCIe Mini Card Slot (for mSATA Modules)

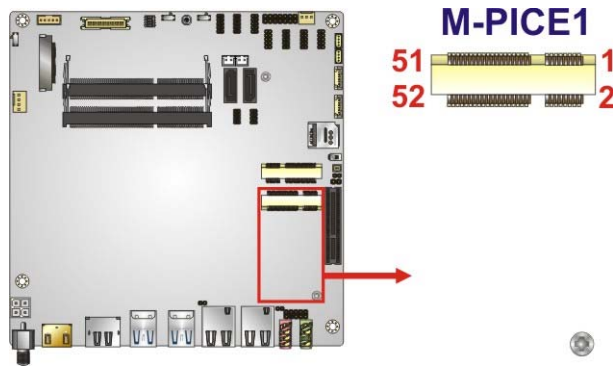
- CN Label:** M-PICE1
- CN Type:** Full-size PCIe Mini card slot
- CN Location:** See **Figure 3-17**
- CN Pinouts:** See **Table 3-16**

The PCIe Mini card slot supports PCIe Mini cards with USB interface, such as mSATA modules.



**NOTE:**

If an mSATA module is installed in the PCIe Mini slot (M-PICE1), the SATA port 2 (SATA2) will be disabled. Choose either the SATA2 connector or the mSATA module for storage.



**Figure 3-17: Full-size PCIe Mini Card Slot Location**

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1   | PCIE_WAKE#  | 2   | +3.3V       |
| 3   | N/C         | 4   | GND         |
| 5   | N/C         | 6   | 1.5 V       |
| 7   | +3.3V       | 8   | N/C         |
| 9   | GND         | 10  | N/C         |

| Pin | Description     | Pin | Description  |
|-----|-----------------|-----|--------------|
| 11  | CLK_PCIE_MINI_N | 12  | N/C          |
| 13  | CLK_PCIE_MINI_P | 14  | N/C          |
| 15  | GND             | 16  | N/C          |
| 17  | BUF_PLT_RST#    | 18  | GND          |
| 19  | N/C             | 20  | +3.3V        |
| 21  | GND             | 22  | BUF_PLT_RST# |
| 23  | PCIE_RXN1       | 24  | +3.3V        |
| 25  | PCIE_RXP1       | 26  | GND          |
| 27  | GND             | 28  | +1.5V        |
| 29  | GND             | 30  | SMB_CLK      |
| 31  | PCIE_TXN1       | 32  | SMB_DATA     |
| 33  | PCIE_TXP1       | 34  | GND          |
| 35  | GND             | 36  | USBD9-       |
| 37  | GND             | 38  | USBD9+       |
| 39  | +3.3V           | 40  | GND          |
| 41  | +3.3V           | 42  | N/C          |
| 43  | GND             | 44  | N/C          |
| 45  | N/C             | 46  | N/C          |
| 47  | N/C             | 48  | +1.5 V       |
| 49  | N/C             | 50  | GND          |
| 51  | MSATA1_DET      | 52  | +3.3V        |

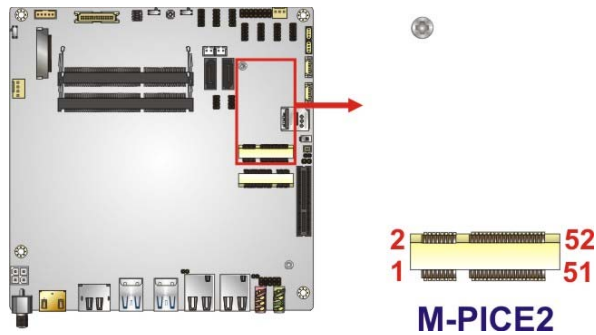
**Table 3-16: PCIe Mini Slot Pinouts (for mSATA Modules)**

### 3.2.17 PCIe Mini Card Slot (for 3G Modules)

- CN Label:** M-PICE2
- CN Type:** Full-size PCIe Mini card slot
- CN Location:** See **Figure 3-18**
- CN Pinouts:** See **Table 3-17**

## tKINO-ULT3 SBC

The PCIe Mini card slot supports PCIe Mini cards with USB interface, such as 3G modules.



**Figure 3-18: Half-size PCIe Mini Slot Location**

| Pin | Description      | Pin | Description  |
|-----|------------------|-----|--------------|
| 1   | PCIE_WAKE#       | 2   | +3.3V        |
| 3   | N/C              | 4   | GND          |
| 5   | N/C              | 6   | +1.5 V       |
| 7   | +3.3V            | 8   | SIM_VCC      |
| 9   | GND              | 10  | SIM_IO       |
| 11  | CLK_PCIE_MINI2_N | 12  | SIM_CLK      |
| 13  | CLK_PCIE_MINI2_P | 14  | SIM_RST      |
| 15  | GND              | 16  | SIM_VPP      |
| 17  | BUF_PLT_RST#     | 18  | GND          |
| 19  | N/C              | 20  | +3.3V        |
| 21  | GND              | 22  | BUF_PLT_RST# |
| 23  | PCIE_RXN5        | 24  | +3.3V        |
| 25  | PCIE_RXP5        | 26  | GND          |
| 27  | GND              | 28  | +1.5 V       |
| 29  | GND              | 30  | SMB_CLK      |
| 31  | PCIE_TXN5        | 32  | SMB_DATA     |
| 33  | PCIE_TXP5        | 34  | GND          |
| 35  | GND              | 36  | USB8-        |
| 37  | GND              | 38  | USB8+        |
| 39  | +3.3V            | 40  | GND          |
| 41  | +3.3V            | 42  | N/C          |

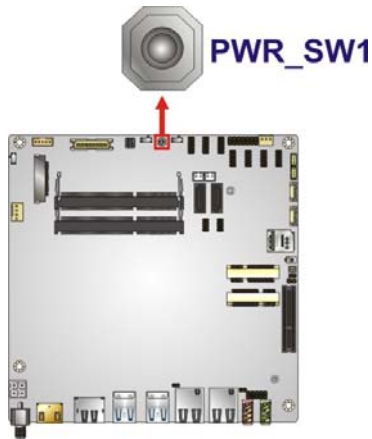
| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 43  | GND         | 44  | N/C         |
| 45  | N/C         | 46  | N/C         |
| 47  | N/C         | 48  | +1.5 V      |
| 49  | N/C         | 50  | GND         |
| 51  | M-SATADET   | 52  | +3.3V       |

**Table 3-17: PCIe Mini Card Slot Pinouts (for 3G Modules)**

### 3.2.18 Power Button

- CN Label:** PWR\_SW1
- CN Type:** Push button
- CN Location:** See **Figure 3-19**

The on-board power button controls system power.



**Figure 3-19: Power Button Location**

tKINO-ULT3 SBC

3.2.19 RS-232 Serial Port Connectors

**CN Label:** COM1, COM2, COM3, COM4

**CN Type:** 10-pin header, p=2.00 mm

**CN Location:** See Figure 3-20

**CN Pinouts:** See Table 3-18

The serial connector provides RS-232 connection.

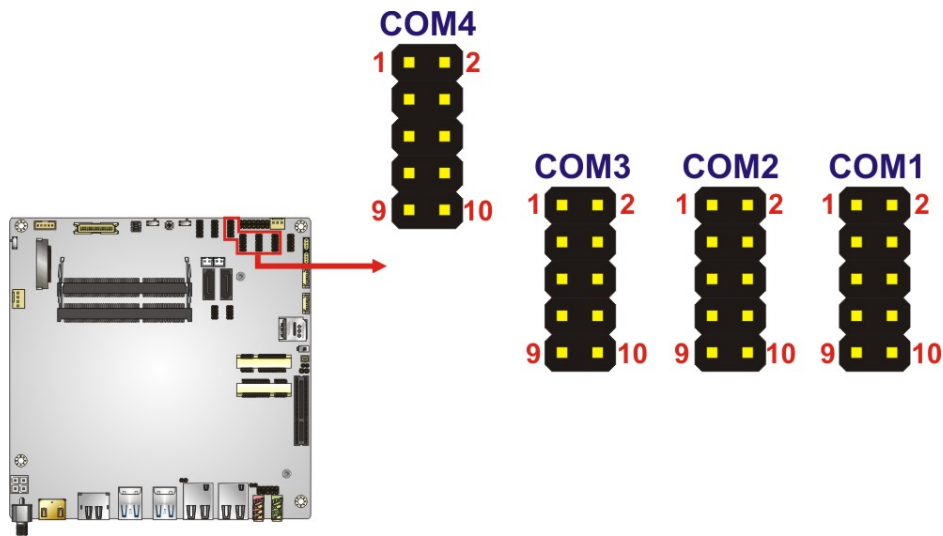


Figure 3-20: RS-232 Serial Port Connector Locations

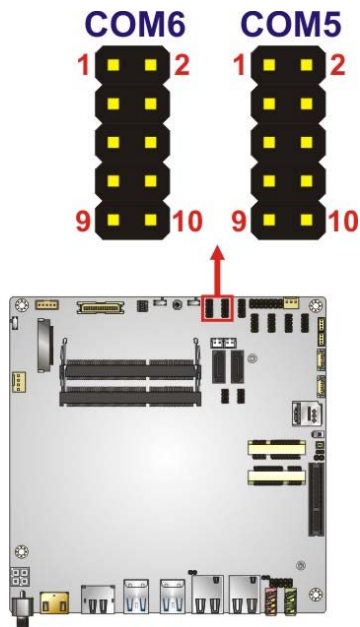
| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1       | DCD         | 2       | DSR         |
| 3       | SIN         | 4       | RTS         |
| 5       | SOUT        | 6       | CTS         |
| 7       | DTR         | 8       | RI          |
| 9       | GND         | 10      | GND         |

Table 3-18: RS-232 Serial Port Connector Pinouts

### 3.2.20 RS-232/422/485 Serial Port Connector

- CN Label:** COM5, COM6
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-21**
- CN Pinouts:** See **Table 3-19**

This connector provides RS-232, RS-422 or RS-485 communications. The default mode is set to RS-232 in BIOS. To configure the connector as RS-422 or RS-485, please refer to **Section 5.3.3.1.5** and **Section 5.3.3.1.6**.



**Figure 3-21: RS-232/422/485 Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1       | DCD         | 2       | DSR         |
| 3       | SIN         | 4       | RTS         |
| 5       | SOUT        | 6       | CTS         |
| 7       | DTR         | 8       | RI          |
| 9       | GND         | 10      | GND         |

**Table 3-19: RS-232/422/485 Connector Pinouts**

tKINO-ULT3 SBC

Use the optional RS-232/422/485 cable to connect to a serial device. The pinouts of the DB-9 connector are listed below.

| RS-232 Pinouts |   | RS-422 Pinouts |   | RS-485 Pinouts |   |
|----------------|---|----------------|---|----------------|---|
| DSR(6)         | 6 | DCD(1)         | 1 | TX-(TXD485#)   | 1 |
| RTS(7)         | 7 | SIN(2)         | 2 | TX+(TXD485+)   | 2 |
| CTS(8)         | 8 | SOUT(3)        | 3 |                | 3 |
| RI(9)          | 9 | DTR(4)         | 4 |                | 4 |
|                |   | GND(5)         | 5 |                | 5 |
|                |   |                |   |                |   |
|                |   |                |   |                |   |
|                |   |                |   |                |   |
|                |   |                |   |                |   |
|                |   |                |   |                |   |

Table 3-20: DB-9 RS-232/422/485 Pinouts

3.2.21 SATA 6Gb/s Drive Connectors

- CN Label:** SATA1, SATA2
- CN Type:** 7-pin SATA connector
- CN Location:** See Figure 3-22

The SATA 6Gb/s drive connector is connected to a SATA 6Gb/s drive. The SATA 6Gb/s drive transfers data at speeds as high as 6Gb/s.

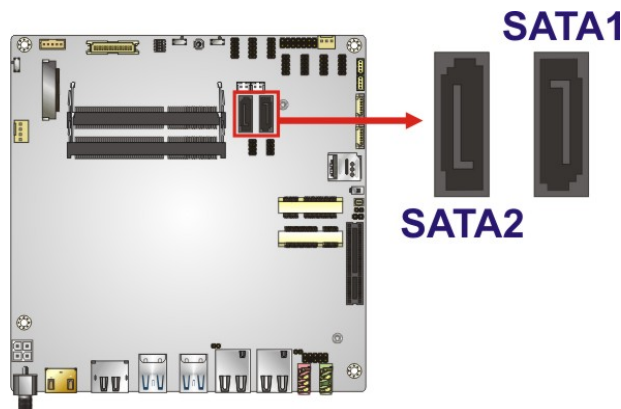


Figure 3-22: SATA 6Gb/s Drive Connectors Locations



**NOTE:**

If an mSATA module is installed in the PCIe Mini slot (M-PICE1), the SATA port 2 (SATA2) will be disabled. Choose either the SATA2 connector or the mSATA module for storage.

**3.2.22 SATA Power Connectors**

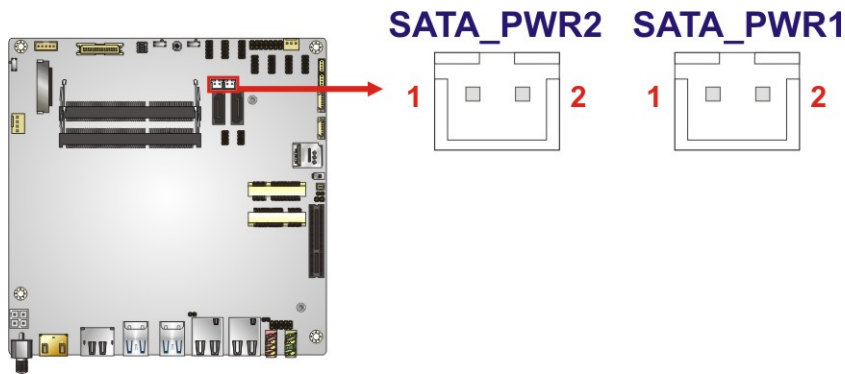
**CN Label:** SATA\_PWR1, SATA\_PWR2

**CN Type:** 2-pin wafer, p=2.00 mm

**CN Location:** See **Figure 3-23**

**CN Pinouts:** See **Table 3-21**

The SATA power connector provides +5 V power output to the SATA connector.



**Figure 3-23: SATA Power Connector Locations**

| Pin | Description |
|-----|-------------|
| 1   | +5V         |
| 2   | GND         |

**Table 3-21: SATA Power Connector Pinouts**

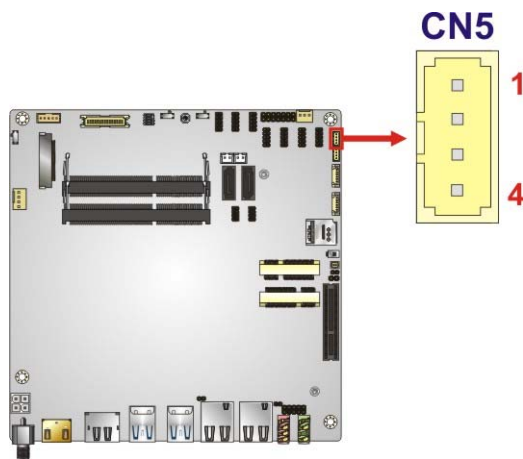


**tKINO-ULT3 SBC**

**3.2.23 SMBus Connector**

- CN Label:** CN5
- CN Type:** 4-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-24**
- CN Pinouts:** See **Table 3-22**

The SMBus (System Management Bus) connector provides low-speed system management communications.



**Figure 3-24: SMBus Connector Location**

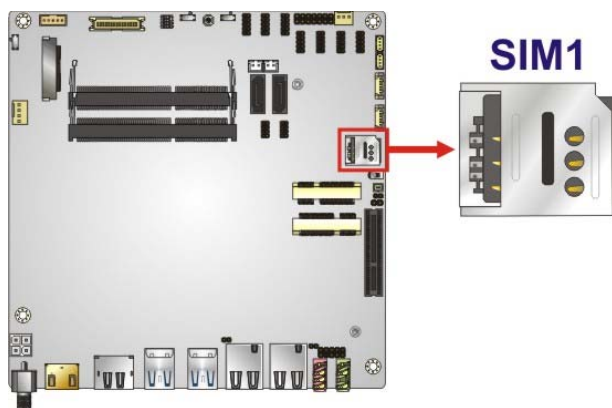
| Pin | Description |
|-----|-------------|
| 1   | GND         |
| 2   | SMB_DATA    |
| 3   | SMB_CLK     |
| 4   | +5V         |

**Table 3-22: SMBus Connector Pinouts**

### 3.2.24 SIM Card Slot

- CN Label:** SIM1
- CN Type:** SIM card slot
- CN Location:** See **Figure 3-25**

The SIM card slot accepts a SIM card for 3G network communication. A 3G module must be installed in the **M-PICE2** PCIe Mini slot to provide 3G communication.



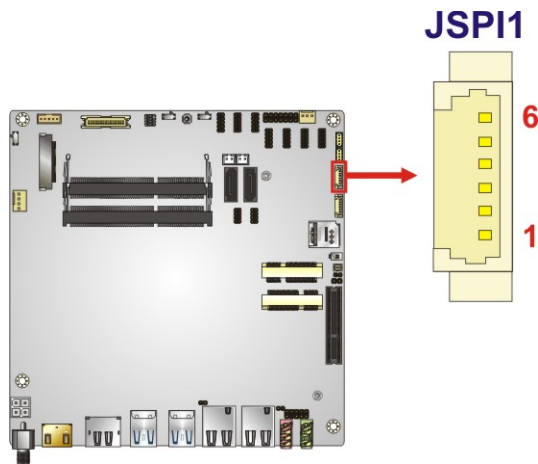
**Figure 3-25: SIM Card Slot Location**

**tKINO-ULT3 SBC**

**3.2.25 SPI Flash Connector, BIOS**

- CN Label:** JSPI1
- CN Type:** 6-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-26**
- CN Pinouts:** See **Table 3-23**

The 6-pin SPI Flash connector is used to flash the BIOS.



**Figure 3-26: SPI Flash Connector Location**

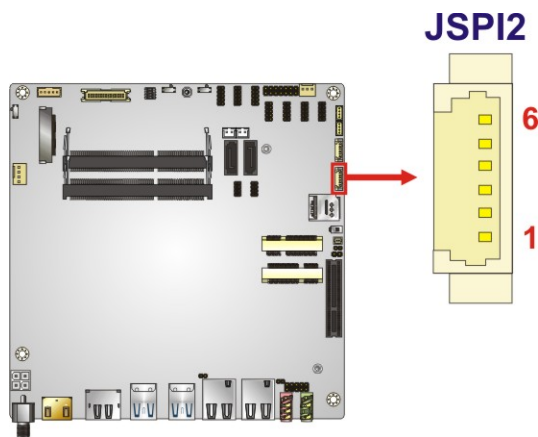
| Pin | Description |
|-----|-------------|
| 1   | +3.3VA      |
| 2   | SPI_CS#     |
| 3   | SPI_SO      |
| 4   | SPI_CLK     |
| 5   | SPI_SI      |
| 6   | GND         |

**Table 3-23: SPI Flash Connector Pinouts**

### 3.2.26 SPI Flash Connector, EC

- CN Label:** JSPI2
- CN Type:** 6-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-27**
- CN Pinouts:** See **Table 3-24**

The 6-pin SPI Flash connector is used to flash the embedded controller.



**Figure 3-27: SPI Flash Connector Location**

| Pin | Description    |
|-----|----------------|
| 1   | +3.3VA         |
| 2   | SPI_CS#0_CN_EC |
| 3   | SPI_SO_SW_EC   |
| 4   | SPI_CLK_SW_EC  |
| 5   | SPI_SI_SW_EC   |
| 6   | GND            |

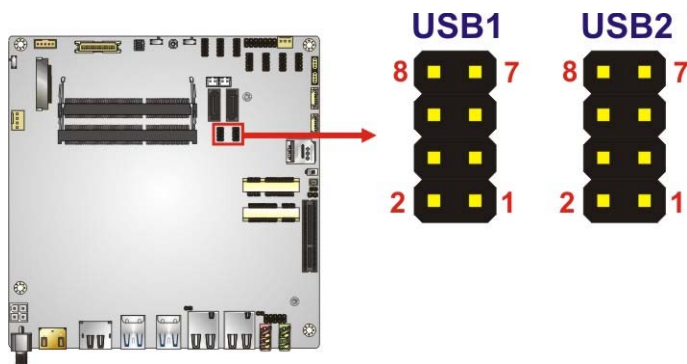
**Table 3-24: SPI Flash Connector Pinouts**

**tKINO-ULT3 SBC**

**3.2.27 USB Connector**

- CN Label:** USB1, USB2
- CN Type:** 8-pin header, p=2.00 mm
- CN Location:** See **Figure 3-28**
- CN Pinouts:** See **Table 3-25**

The USB connector provides two USB 2.0 ports by dual-port USB cable.



**Figure 3-28: USB Connector Location**

| PIN NO. | DESCRIPTION | PIN NO. | DESCRIPTION |
|---------|-------------|---------|-------------|
| 1       | VCC         | 2       | GND         |
| 3       | DATA-       | 4       | DATA+       |
| 5       | DATA+       | 6       | DATA-       |
| 7       | GND         | 8       | VCC         |

**Table 3-25: USB Connector Pinouts**

### 3.3 External Peripheral Interface Connector Panel

Figure 3-29 shows the tKINO-ULT3 external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

- 1 x Audio line-out jack
- 1 x Audio mic-in jack
- 2 x GbE connector
- 1 x HDMI connector
- 1 x HDMI/DP combo connector
- 1 x Power input jack
- 4 x USB 3.0 connector

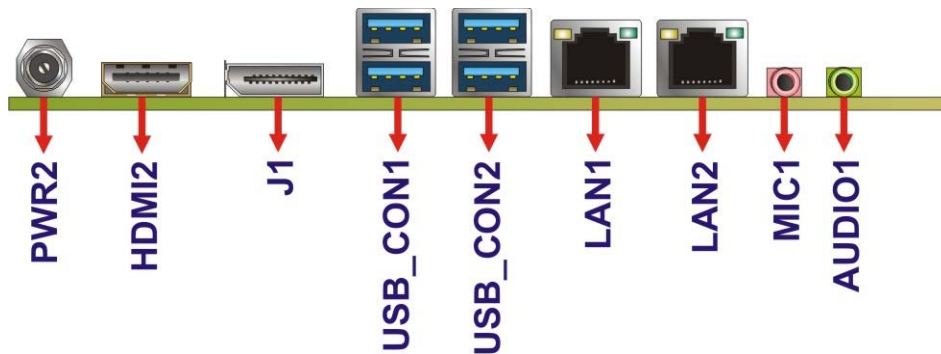


Figure 3-29: External Peripheral Interface Connector

#### 3.3.1 Audio Jacks

|              |                 |
|--------------|-----------------|
| CN Label:    | AUDIO1, MIC1    |
| CN Type:     | Audio jacks     |
| CN Location: | See Figure 3-29 |

The audio jacks connect to external audio devices.

- **Line Out port (Lime):** Connects to a headphone or a speaker. With multi-channel configurations, this port can also connect to front speakers.
- **Microphone (Pink):** Connects a microphone.

**tKINO-ULT3 SBC**

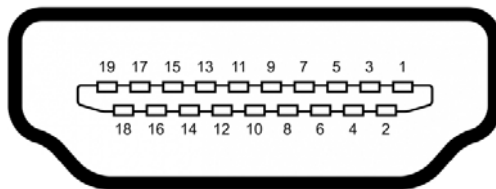
**3.3.2 HDMI Connector**

- CN Label:** HDMI2
- CN Type:** HDMI connector
- CN Location:** See **Figure 3-29**
- CN Pinouts:** See **Table 3-26**

The HDMI connector can connect to HDMI devices.

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1   | HDMI_DATA2  | 2   | GND         |
| 3   | HDMI_DATA2# | 4   | HDMI_DATA1  |
| 5   | GND         | 6   | HDMI_DATA1# |
| 7   | HDMI_DATA0  | 8   | GND         |
| 9   | HDMI_DATA0# | 10  | HDMI_CLK    |
| 11  | GND         | 12  | HDMI_CLK#   |
| 13  | N/C         | 14  | N/C         |
| 15  | HDMI_SCL    | 16  | HDMI_SDA    |
| 17  | GND         | 18  | +5V         |
| 19  | HDMI_HPD    | 20  | HDMI_GND    |
| 21  | HDMI_GND    | 22  | HDMI_GND    |
| 23  | HDMI_GND    |     |             |

**Table 3-26: HDMI Connector Pinouts**



**Figure 3-30: HDMI Connector Pinout Locations**

### 3.3.3 HDMI/DP Combo Connector

- CN Label:** J1
- CN Type:** HDMI/DP combo connector
- CN Location:** See **Figure 3-29**
- CN Pinouts:** See **Table 3-27**

The HDMI/DP connector can connect to display devices with HDMI or DisplayPort interface. The mode selection is made through a switch (J\_HDMI\_DP1) on the board (refer to **Section 4.6.4** for detailed information). The connector is set to HDMI by default.

| Pin | HDMI           | DisplayPort    |
|-----|----------------|----------------|
| 1   | TMDS DATA2+    | LOP            |
| 2   | GND            | GND            |
| 3   | TMDS DATA2-    | L0N            |
| 4   | TMDS DATA1+    | L1P            |
| 5   | GND            | GND            |
| 6   | TMDS DATA1-    | L1N            |
| 7   | TMDS DATA0+    | L2P            |
| 8   | GND            | GND            |
| 9   | TMDS DATA0-    | L2N            |
| 10  | TMDS CLK+      | L3P            |
| 11  | GND            | GND            |
| 12  | TMDS CLK+      | L3N            |
| 13  | CEC            | GND            |
| 14  | NC             | GND            |
| 15  | SCL            | AUXP           |
| 16  | SDA            | GND            |
| 17  | GND            | AUXN           |
| 18  | HDMI PWR       | HPD            |
| 19  | HPD            | PWR RTN        |
| 20  | NC             | DP PWR         |
| 21  | HDMI/DP detect | HDMI/DP detect |

**Table 3-27: HDMI/DP Combo Connector Pinouts**



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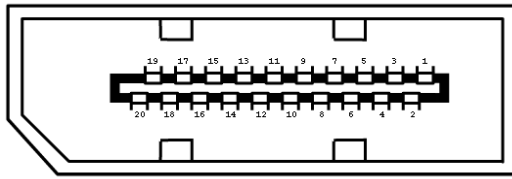


Figure 3-31: HDMI/DP Combo Connector Pinout Locations

### 3.3.4 LAN Connectors

- CN Label:** LAN1, LAN2
- CN Type:** RJ-45
- CN Location:** See Figure 3-29
- CN Pinouts:** See Figure 3-32 and Table 3-28

The LAN connector connects to a local network.

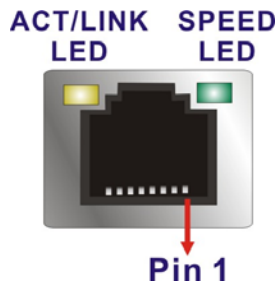


Figure 3-32: LAN Connector

| Pin | Description | Pin | Description |
|-----|-------------|-----|-------------|
| 1   | TRD0+       | 5   | TRD2+       |
| 2   | TRD0-       | 6   | TRD2-       |
| 3   | TRD1+       | 7   | TRD3+       |
| 4   | TRD1-       | 8   | TRD3-       |

Table 3-28: LAN Pinouts

### 3.3.5 Power Connector (Power Adapter)

- CN Label:** PWR2
- CN Type:** DC jack
- CN Location:** See **Figure 3-29**

The connector supports 9 V ~ 36 V power adapter.



**Figure 3-33: Power Jack**

### 3.3.6 USB 3.0 Connectors

- CN Label:** USB\_CON1, USB\_CON2
- CN Type:** USB 3.0 port
- CN Location:** See **Figure 3-29**
- CN Pinouts:** See **Table 3-29**

The tKINO-ULT3 has four external USB 3.0 ports. The USB connector can be connected to a USB 2.0 or USB 3.0 device. The pinouts of USB 3.0 connectors are shown below.

| Pin | Description  | Pin | Description  |
|-----|--------------|-----|--------------|
| 1   | +5V          | 2   | USB2P0-      |
| 3   | USB2P0+      | 4   | GND          |
| 5   | USB3P0_RXDN1 | 6   | USB3P0_RXDP1 |
| 7   | GND          | 8   | USB3P0_TXDN1 |
| 9   | USB3P0_TXDP1 |     |              |

**Table 3-29: USB 3.0 Port Pinouts**

Chapter

4

# Installation

---

## 4.1 Anti-static Precautions

---



### WARNING:

Failure to take ESD precautions during the installation of the tKINO-ULT3 may result in permanent damage to the tKINO-ULT3 and severe injury to the user.

---

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the tKINO-ULT3. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the tKINO-ULT3 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- **Wear an anti-static wristband:** Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- **Self-grounding** Before handling the board, touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- **Use an anti-static pad:** When configuring the tKINO-ULT3, place it on an anti-static pad. This reduces the possibility of ESD damaging the tKINO-ULT3.
- **Only handle the edges of the PCB:** When handling the PCB, hold the PCB by the edges.

## 4.2 Installation Considerations

---



### NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

---

**WARNING:**

The installation instructions described in this manual should be carefully followed in order to prevent damage to the tKINO-ULT3, tKINO-ULT3 components and injury to the user.

Before and during the installation please **DO** the following:

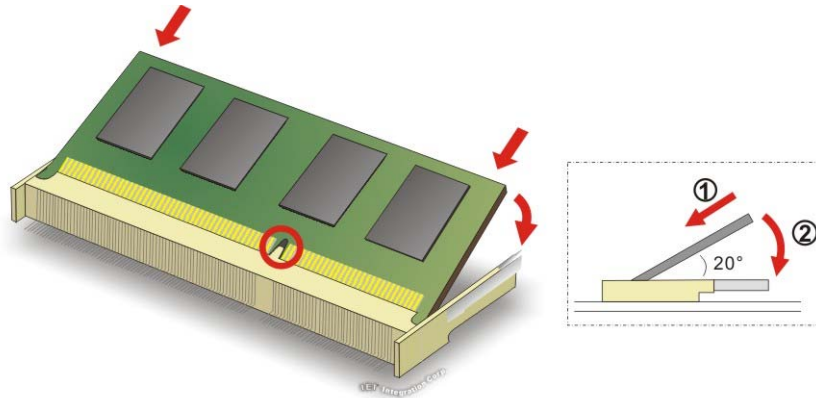
- Read the user manual:
  - The user manual provides a complete description of the tKINO-ULT3 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
  - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the tKINO-ULT3 on an antistatic pad:
  - When installing or configuring the motherboard, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn all power to the tKINO-ULT3 off:
  - When working with the tKINO-ULT3, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the tKINO-ULT3 **DO NOT**:

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

### 4.3 SO-DIMM Installation

To install an SO-DIMM, please follow the steps below and refer to **Figure 4-1**.



**Figure 4-1: SO-DIMM Installation**

- Step 1:** Locate the **SO-DIMM socket**. Place the board on an anti-static mat.
- Step 2:** **Align the SO-DIMM with the socket**. Align the notch on the memory with the notch on the memory socket.
- Step 3:** **Insert the SO-DIMM**. Push the memory in at a 20° angle. (See **Figure 4-1**)
- Step 4:** **Seat the SO-DIMM**. Gently push downwards and the arms clip into place. (See **Figure 4-1**)

### 4.4 PCIe Mini Card Installation

To install a full-size PCIe Mini card, please follow the steps below.

- Step 1:** **Locate the full-size PCIe Mini card slot**. See **Chapter 3**.
- Step 2:** **Remove the retention screw**. Remove the retention screw as shown in **Figure 4-2**.

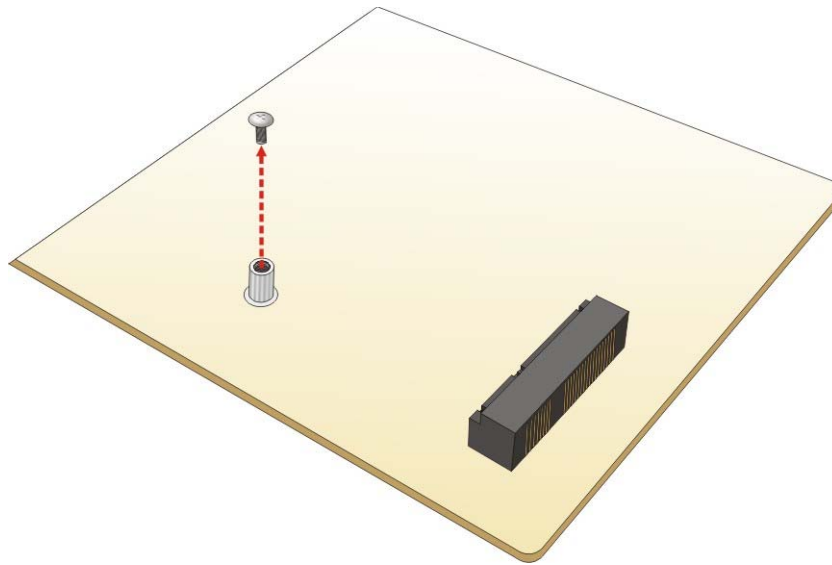


Figure 4-2: Removing the Retention Screw

**Step 3:** Insert into the socket at an angle. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the socket at an angle of about 20° (Figure 4-3).

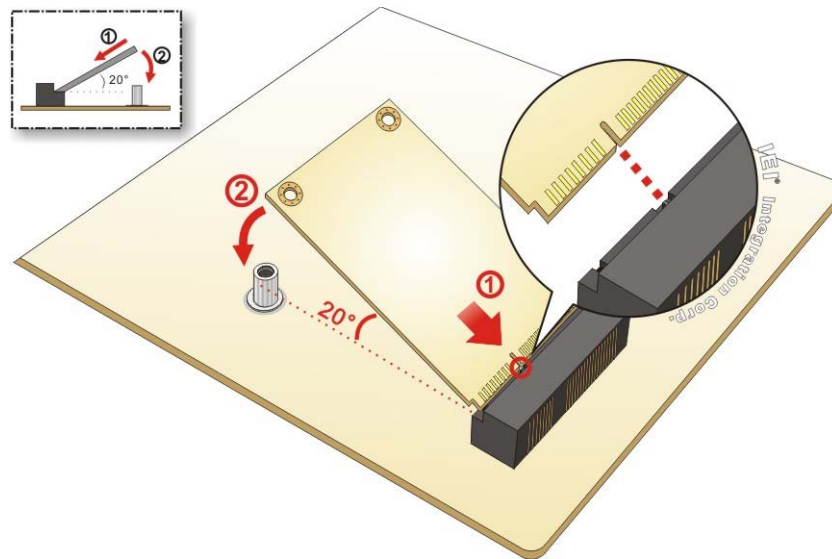


Figure 4-3: Inserting the Full-size PCIe Mini Card into the Slot at an Angle

**Step 4:** Secure the full-size PCIe Mini card. Secure the full-size PCIe Mini card with the retention screw previously removed (Figure 4-4).

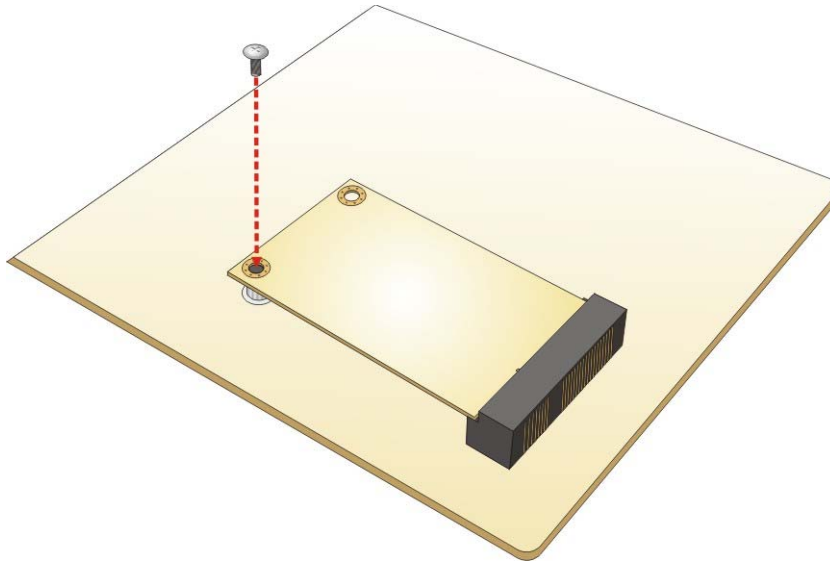


Figure 4-4: Securing the Full-size PCIe Mini Card

## 4.5 SIM Card Installation

To install a SIM card, please follow the steps below.

**Step 1:** Locate the SIM card slot. See **Section 3.2.24**.

**Step 2:** Unlock the SIM card slot cover by sliding the cover in the direction as shown by the arrow in **Figure 4-5**.

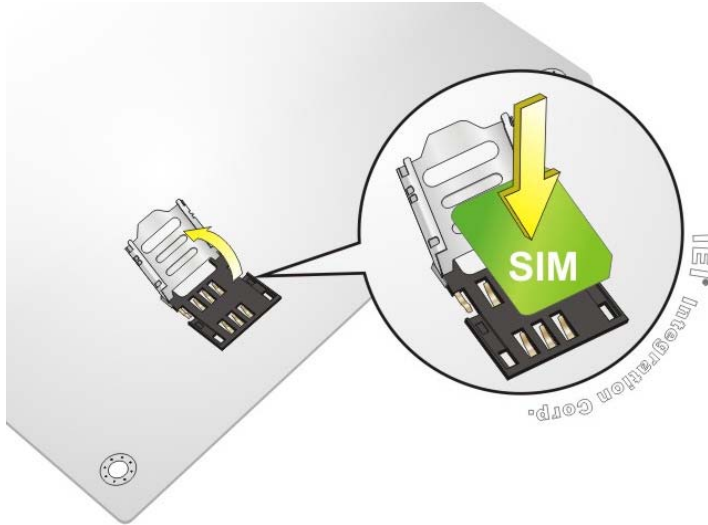


Figure 4-5: Unlock SIM Card Slot Cover



## tKINO-ULT3 SBC

**Step 3:** Open the slot cover and place a SIM card onto the slot. The cut mark on the corner should be facing away from the slot as shown in **Figure 4-6**.



**Figure 4-6: SIM Card Installation**

**Step 4:** Close the slot cover and lock it by sliding it in the direction as shown by the arrow in **Figure 4-7**.



**Figure 4-7: Lock SIM Card Slot Cover**

## 4.6 System Configuration

The system configuration is controlled by buttons, jumpers and switches. The system configuration should be performed before installation.

### 4.6.1 AT/ATX Mode Select Switch

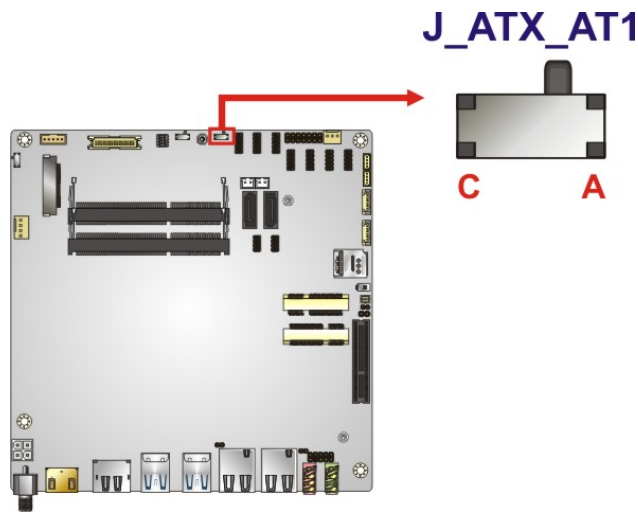
|                     |                       |
|---------------------|-----------------------|
| <b>CN Label:</b>    | <b>J_ATX_AT1</b>      |
| <b>CN Type:</b>     | Switch                |
| <b>CN Location:</b> | See <b>Figure 4-8</b> |
| <b>CN Settings:</b> | See <b>Table 4-1</b>  |

The AT/ATX mode select switch specifies the systems power mode as AT or ATX. AT/ATX mode select switch settings are shown in **Table 4-1**.

| Setting   | Description        |
|-----------|--------------------|
| Short A-B | ATX Mode (Default) |
| Short B-C | AT Mode            |

**Table 4-1: AT/ATX Mode Select Switch Settings**

The location of the AT/ATX mode select switch is shown in **Figure 4-8** below.



**Figure 4-8: AT/ATX Mode Select Switch Location**

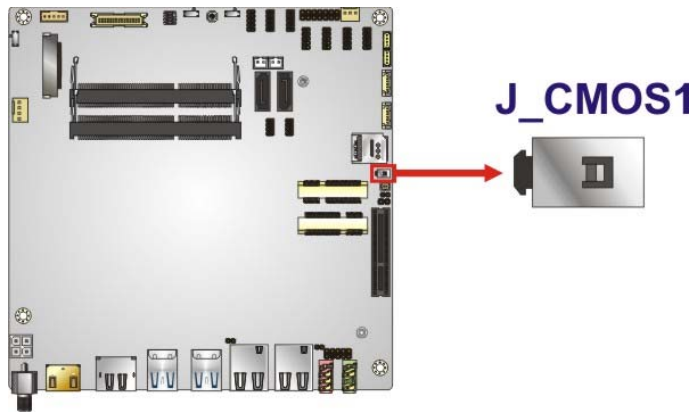
## tKINO-ULT3 SBC

### 4.6.2 Clear CMOS Button

|                     |                       |
|---------------------|-----------------------|
| <b>CN Label:</b>    | <b>J_CMOS1</b>        |
| <b>CN Type:</b>     | Button                |
| <b>CN Location:</b> | See <b>Figure 4-9</b> |

If the tKINO-ULT3 fails to boot due to improper BIOS settings, use the button to clear the CMOS data and reset the system BIOS information.

The location of the clear CMOS button is shown in **Figure 4-9**



**Figure 4-9: Clear CMOS Button Location**

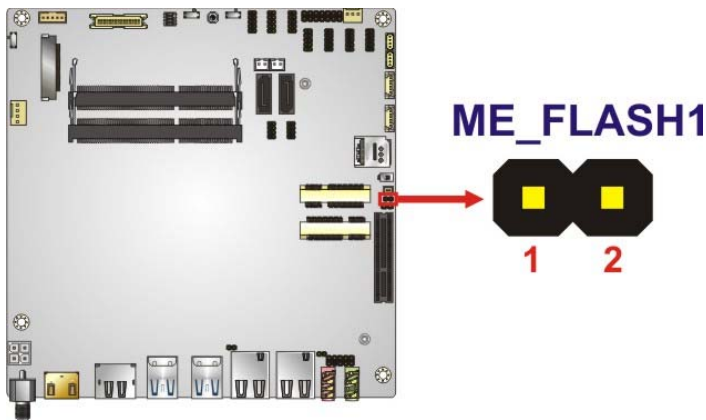
### 4.6.3 Flash Descriptor Security Override Jumper

|                     |                         |
|---------------------|-------------------------|
| <b>CN Label:</b>    | <b>ME_FLASH1</b>        |
| <b>CN Type:</b>     | 2-pin header, p=2.00 mm |
| <b>CN Location:</b> | See <b>Figure 4-10</b>  |
| <b>CN Settings:</b> | See <b>Table 4-2</b>    |

The Flash Descriptor Security Override jumper (ME\_FLASH1) allows to enable or disable the ME firmware update. Refer to **Figure 4-10** and **Table 4-2** for the jumper location and settings.

| Setting | Description        |
|---------|--------------------|
| Open    | Disabled (default) |
| Short   | Enabled            |

**Table 4-2: Flash Descriptor Security Override Jumper Settings**



**Figure 4-10: Flash Descriptor Security Override Jumper Location**

To update the ME firmware, please follow the steps below.

- Step 1:** Before turning on the system power, short the Flash Descriptor Security Override jumper.
- Step 2:** Update the BIOS and ME firmware, and then turn off the system power.
- Step 3:** Remove the metal clip on the Flash Descriptor Security Override jumper to its default setting.
- Step 4:** Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update.

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4.6.4 HDMI/DP Select Switch

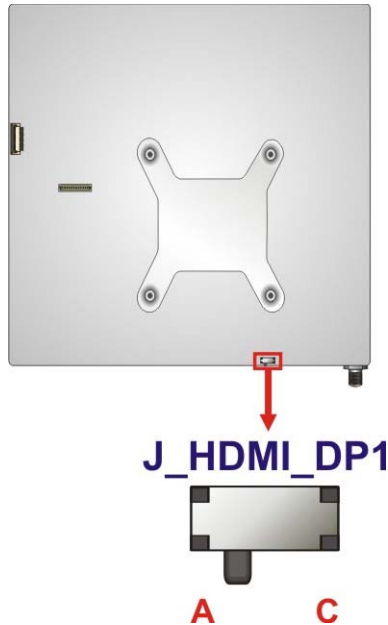
- CN Label:** J\_HDMI\_DP1
- CN Type:** Switch
- CN Location:** See **Figure 4-11**
- CN Settings:** See **Table 4-3**

Use the HDMI/DP select switch to configure the HDMI/DP connector as HDMI or DisplayPort. HDMI/DP select switch settings are shown in **Table 4-3**.

| Setting   | Description         |
|-----------|---------------------|
| Short A-B | HDMI mode (Default) |
| Short B-C | DisplayPort mode    |

**Table 4-3: HDMI/DP Select Switch Settings**

The location of the HDMI/DP select switch is shown in **Figure 4-11** below.



**Figure 4-11: HDMI/DP Select Switch Location**

### 4.6.5 LVDS/eDP Select Switch

- CN Label:** J\_EDP\_SEL1
- CN Type:** Switch
- CN Location:** See **Figure 4-12**
- CN Settings:** See **Table 4-4**

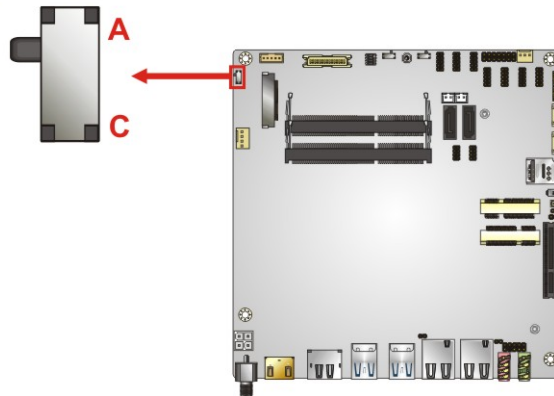
Use the LVDS/eDP select switch to disable or enable the LVDS connector since the eDP connector (CN10) is co-lay with the LVDS connector. LVDS/eDP select switch settings are shown in **Table 4-4**.

| Setting   | Description         |
|-----------|---------------------|
| Short A-B | LVDS mode (Default) |
| Short B-C | eDP mode            |

**Table 4-4: LVDS/eDP Select Switch Settings**

The location of the LVDS/eDP select switch is shown in **Figure 4-12** below.

#### J\_EDP\_SEL1



**Figure 4-12: LVDS/eDP Select Switch Location**

### 4.6.6 LVDS Panel Resolution Select Switch

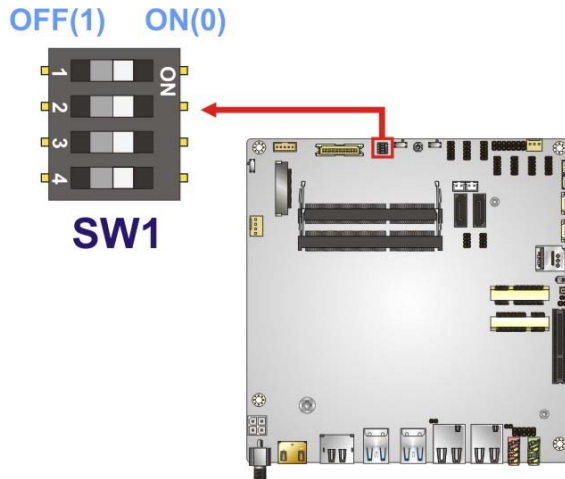
- Jumper Label:** SW1
- Jumper Type:** DIP switch
- Jumper Location:** See **Figure 4-13**
- Jumper Settings:** See **Table 4-5**

Selects the resolution of the LCD panel connected to the LVDS connector.

\* ON=0, OFF=1

| <b>SW1 (4-3-2-1)</b> | <b>Description</b>       |
|----------------------|--------------------------|
| 0000                 | 800x600 18-bit (default) |
| 0001                 | 1024x768 18-bit          |
| 0010                 | 1024x768 24-bit          |
| 0011                 | 1280x768 18-bit          |
| 0100                 | 1280x800 18-bit          |
| 0101                 | 1280x960 18-bit          |
| 0110                 | 1280x1024 48-bit         |
| 0111                 | 1366x768 18-bit          |
| 1000                 | 1366x768 24-bit          |
| 1001                 | 1440x900 48-bit          |
| 1010                 | 1400x1050 48-bit         |
| 1011                 | 1600x900 48-bit          |
| 1100                 | 1680x1050 48-bit         |
| 1101                 | 1600x1200 48-bit         |
| 1110                 | 1920x1080 48-bit         |
| 1111                 | 1920x1200 48-bit         |

**Table 4-5: LVDS Panel Resolution Selection**



**Figure 4-13: LVDS Panel Resolution Select Switch Location**

#### 4.6.7 LVDS Voltage Select Switch



**WARNING:**

Permanent damage to the screen and tKINO-ULT3 may occur if the wrong voltage is selected with this jumper. Please refer to the user guide that came with the monitor to select the correct voltage.

- Jumper Label:** J\_LCD\_PWR1
- Jumper Type:** Switch
- Jumper Settings:** See Table 4-6
- Jumper Location:** See Figure 4-14

The LVDS voltage select switch allows setting the voltage provided to the monitor connected to the LVDS connector. Refer to **Figure 4-14** and **Table 4-6** for the jumper location and settings.

| Setting   | Description      |
|-----------|------------------|
| Short A-B | +3.3 V (Default) |
| Short B-C | +5               |

**Table 4-6: LVDS Voltage Select Switch Settings**



J\_LCD\_PWR1

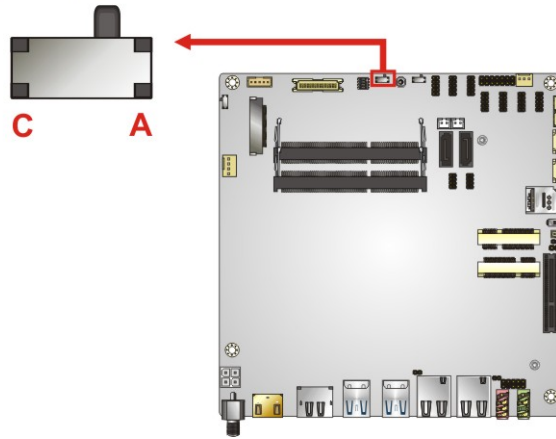


Figure 4-14: LVDS Voltage Select Switch Location

#### 4.6.8 USB Power Select

The USB power selection is made through the BIOS options in “Chipset → PCH-IO Configuration” BIOS menu. Use the **USB Power SW** BIOS option to configure the power source to all the external and internal USB ports of the tKINO-ULT3.

|   |          |         |                                      |
|---|----------|---------|--------------------------------------|
| ➔ | +5V DUAL | DEFAULT | Set the USB power source to +5V dual |
| ➔ | +5V      |         | Set the USB power source to +5V      |

Table 4-7: USB Power Selection BIOS Options

Please refer to **Section 5.4.2** for detailed information.

## 4.7 Chassis Installation

### 4.7.1 Airflow



#### **WARNING:**

Airflow is critical for keeping components within recommended operating temperatures. The chassis should have fans and vents as necessary to keep things cool.

---

The tKINO-ULT3 must be installed in a chassis with ventilation holes on the sides allowing airflow to travel through the heat sink surface. In a system with an individual power supply unit, the cooling fan of a power supply can also help generate airflow through the board surface.

### 4.7.2 Motherboard Installation

To install the tKINO-ULT3 motherboard into the chassis please refer to the reference material that came with the chassis.

## 4.8 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the on-board connectors

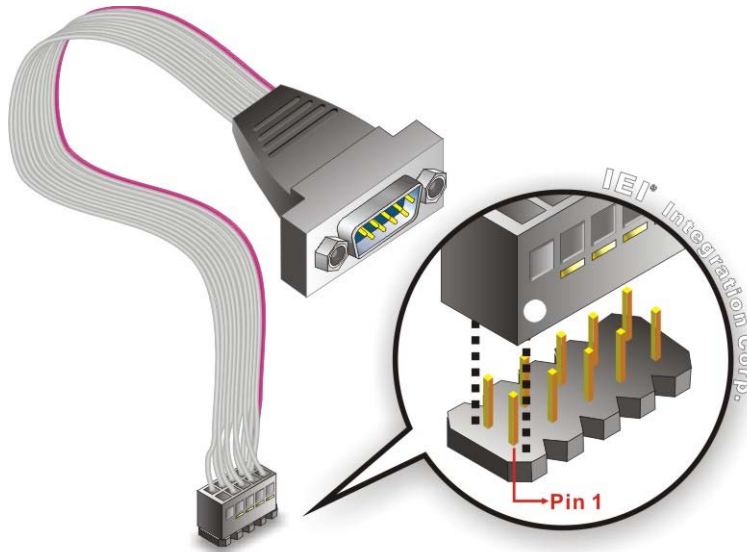
### 4.8.1 RS-232 Cable Connection

The single RS-232 cable consists of one serial port connector attached to a serial communications cable that is then attached to a D-sub 9 male connector. To install the single RS-232 cable, please follow the steps below.

**Step 1:** **Locate the connector.** The location of the RS-232 connector is shown in **Chapter 3.**

## tKINO-ULT3 SBC

- Step 2:** **Insert the cable connector.** Align the cable connector with the onboard connector. Make sure pin 1 on the board and connector line up. Pin 1 on the cable connector is indicated with a white dot. See **Figure 4-15**.



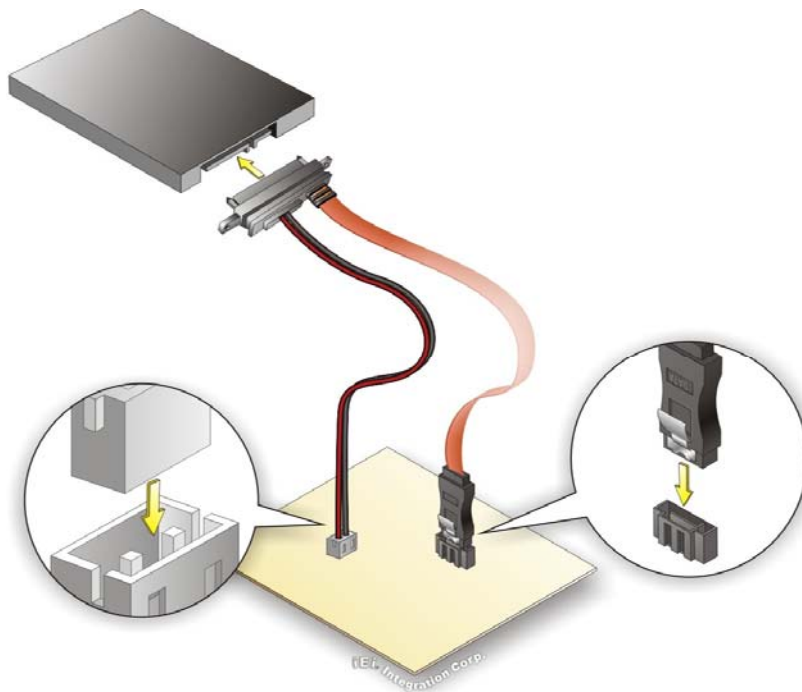
**Figure 4-15: Single RS-232 Cable Installation**

- Step 3:** **Secure the bracket.** The single RS-232 connector has two retention screws that must be secured to a chassis or bracket.
- Step 4:** **Connect the serial device.** Once the single RS-232 connector is connected to a chassis or bracket, a serial communications device can be connected to the system.

### 4.8.2 SATA Drive Connection

The tKINO-ULT3 is shipped with a SATA drive cable. To connect the SATA drive to the connector, please follow the steps below.

- Step 1:** **Locate the SATA connector and the SATA power connector.** The locations of the connectors are shown in **Chapter 3**.
- Step 2:** **Insert the cable connector.** Insert the cable connector into the on-board SATA drive connector and the SATA power connector. See **Figure 4-16**.



**Figure 4-16: SATA Drive Cable Connection**

- Step 3:** **Connect the cable to the SATA disk.** Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-16**.
- Step 4:** To remove the SATA cable from the SATA connector, press the clip on the connector at the end of the cable.

## 4.9 Intel® AMT Setup Procedure

The tKINO-ULT3 is featured with the Intel® Active Management Technology (AMT). To enable the Intel® AMT function, follow the steps below.

- Step 1:** Make sure at least one of the memory sockets is installed with a DDR4 SO-DIMM.
- Step 2:** Connect an Ethernet cable to the RJ-45 connector labeled **LAN1**.
- Step 3:** The AMI BIOS options regarding the Intel® ME or Intel® AMT must be enabled,
- Step 4:** Properly install the Intel® Management Engine Components drivers from the Intel AMT (ME) directory in the driver CD.
- Step 5:** Configure the Intel® Management Engine BIOS extension (MEBx). To get into the Intel® MEBx settings, press <Ctrl+P> after a single beep during boot-up process. Enter the Intel® current ME password as it requires (the Intel® default password is **admin**).



### NOTE:

To change the password, enter a new password following the strong password rule (containing at least one upper case letter, one lower case letter, one digit and one special character, and be at least eight characters).

---

Chapter

**5**

# **BIOS**

---

## 5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.



### NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

### 5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DELETE** or **F2** key as soon as the system is turned on or
2. Press the **DELETE** or **F2** key when the “**Press Del to enter SETUP**” message appears on the screen.

If the message disappears before the **DELETE** or **F2** key is pressed, restart the computer and try again.

### 5.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **ESC** to quit. Navigation keys are shown in.

| Key         | Function                                   |
|-------------|--|
| Up arrow    | Move to previous item                      |
| Down arrow  | Move to next item                          |
| Left arrow  | Move to the item on the left hand side     |
| Right arrow | Move to the item on the right hand side    |
| +           | Increase the numeric value or make changes |

| Key     | Function   |
|---------|--|
| -       | Decrease the numeric value or make changes   |
| F1 key  | General help, only for Status Page Setup Menu and Option Page Setup Menu   |
| F2 key  | Load previous values.  |
| F3 key  | Load optimized defaults  |
| F4 key  | Save changes and Exit BIOS   |
| Esc key | Main Menu – Quit and not save changes into CMOS<br>Status Page Setup Menu and Option Page Setup Menu --<br>Exit current page and return to Main Menu |

### 5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window press **Esc** or the **F1** key again.

### 5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the jumper described in **Section 4.6.2**.

### 5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.



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### 5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered.

| Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc. |   |         |              |      |  |
|--|---|---------|--------------|------|--|
| Main   | Advanced                                    | Chipset | Security     | Boot | Save & Exit  |
| BIOS Information   |   |         |              |      |  |
| BIOS Vendor  | American Megatrends                         |         |              |      | Set the Date. Use Tab to switch between Data elements. |
| Core Version   | 5.11  |         |              |      |  |
| Compliancy   | UEFI 2.4; PI 1.3                            |         |              |      |  |
| Project Version  | B398AR11.ROM                                |         |              |      |  |
| Build Date and Time  | 03/14/2017 10:21:28                         |         |              |      |  |
| iWDD Vendor  |   |         | iEi          |      |  |
| iWDD Version   |   |         | B398ER11.bin |      |  |
| Processor Information  |   |         |              |      |  |
| Name   | SkyLake                                     |         |              |      |  |
| Brand String   | Intel(R) Core(TM)<br>i3-6100U CPU @ 2.30GHz |         |              |      |  |
| Frequency  | 2200 MHz                                    |         |              |      | -----  |
| Processor ID   | 406E3                                       |         |              |      | ←→: Select Screen                                      |
| Stepping   | D0/K0                                       |         |              |      | ↑ ↓: Select Item                                       |
| Number of Processors   | 2Core(s) / 4Thread(s)                       |         |              |      | EnterSelect  |
| Microcode Revision   | 7C  |         |              |      | +/-: Change Opt.                                       |
| GT Info  | GT1   |         |              |      | F1: General Help                                       |
| IGFX VBIOS Version   | 1040  |         |              |      | F2: Previous Values                                    |
| Memory RC Version  | 1.9.0.0                                     |         |              |      | F3: Optimized Defaults                                 |
| Total Memory   | 4096 MB                                     |         |              |      | F4: Save & Exit  |
| Memoery Frequency  | 2133 MHz                                    |         |              |      | ESC: Exit  |
| PCH Information  |   |         |              |      |  |
| Name   | SKL PCH-LP                                  |         |              |      |  |
| PCH SKU  | PCH-LP Mobile (U)<br>Premium SKU            |         |              |      |  |
| Stepping   | 21/C1                                       |         |              |      |  |
| LAN PHY Revision   | B2  |         |              |      |  |
| ME FW Version  | 11.0.0.1202                                 |         |              |      |  |
| ME Firmware SKU  | Corporate SKU                               |         |              |      |  |
| SPI Clock Frequency  |   |         |              |      |  |
| D0FR Support   | Unsupported                                 |         |              |      |  |
| Read Status Clock Frequency  | 17 MHz                                      |         |              |      |  |
| Write Status Clock Frequency                                       | 17 MHz                                      |         |              |      |  |
| Fast Read Status Clock Frequency                                   | 17 MHz                                      |         |              |      |  |
| System Date  | [Fri 01/01/2010]                            |         |              |      |  |
| System Time  | [00:18:35]                                  |         |              |      |  |
| Version 2.17.1255. Copyright (C) 2017 American Megatrends, Inc.    |   |         |              |      |  |

**BIOS Menu 1: Main**

The System Overview field also has two user configurable fields:

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

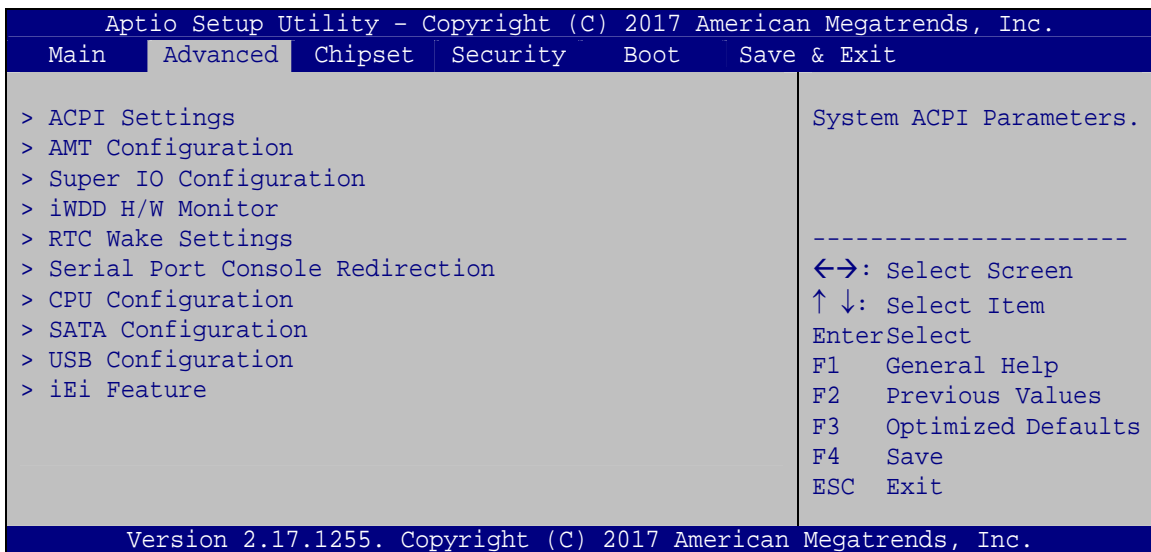
### 5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:



**WARNING!**

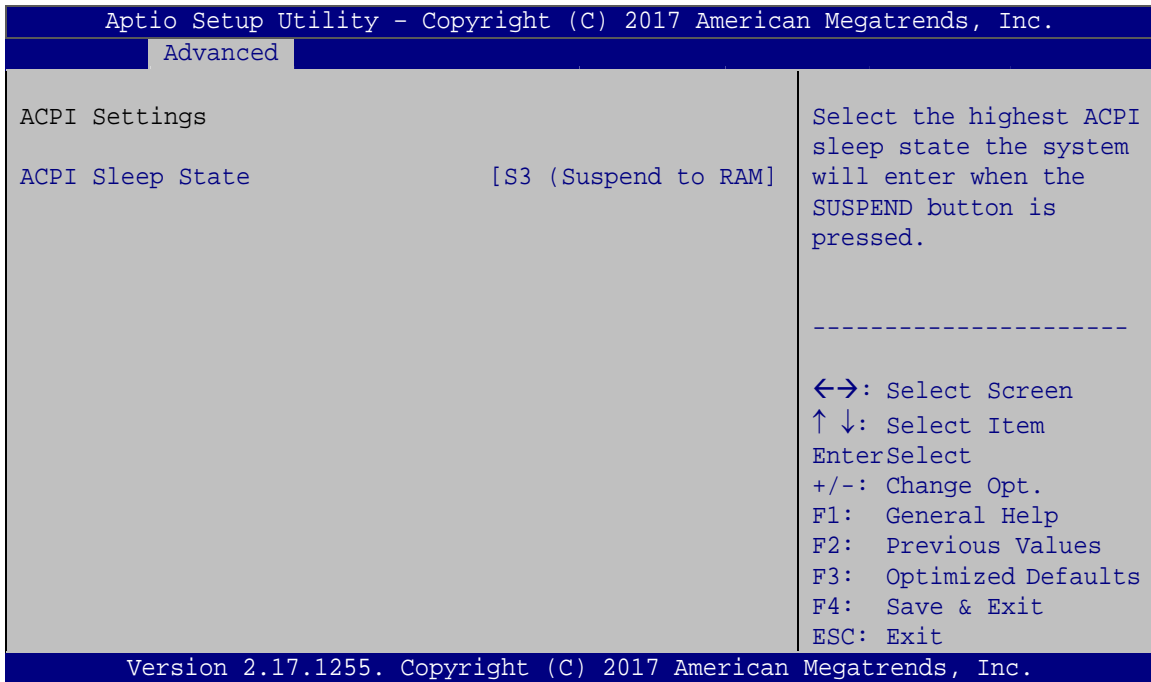
Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.



**BIOS Menu 2: Advanced**

### 5.3.1 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 3**) configures the Advanced Configuration and Power Interface (ACPI) options.



#### **BIOS Menu 3: ACPI Settings**

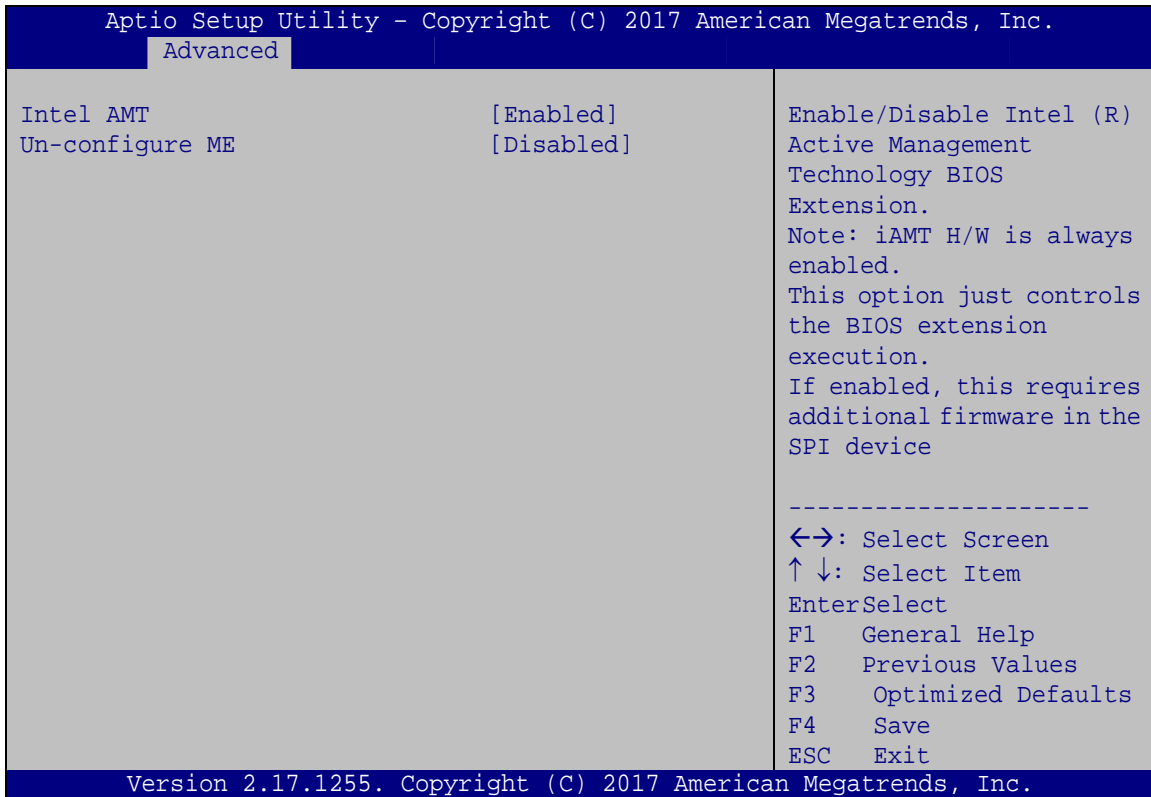
##### → **ACPI Sleep State [S3 (Suspend to RAM)]**

Use the **ACPI Sleep State** option to specify the sleep state the system enters when it is not being used.

- **S3 (Suspend to RAM)**    **DEFAULT**    The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

### 5.3.2 AMT Configuration

The **AMT Configuration** menu (**BIOS Menu 4**) allows Intel® Active Management Technology (AMT) options to be configured.



#### BIOS Menu 4: AMT Configuration

##### → Intel AMT [Enabled]

Use **Intel AMT** option to enable or disable the Intel® AMT function.

- **Disabled** Intel® AMT is disabled
- **Enabled** **DEFAULT** Intel® AMT is enabled

##### → Un-configure ME [Disabled]

Use the **Un-configure ME** option to perform ME unconfigure without password operation.

- **Disabled** **DEFAULT** Not perform ME unconfigure

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➔ Enabled To perform ME unconfigure

### 5.3.3 Super IO Configuration

Use the **Super IO Configuration** menu (**BIOS Menu 5**) to set or change the configurations for the serial ports.

```

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.
  Advanced
-----
Super IO Configuration
Super IO Chip                F81866
> Serial Port 1 Configuration
> Serial Port 2 Configuration
> Serial Port 3 Configuration
> Serial Port 4 Configuration
> Serial Port 5 Configuration
> Serial Port 6 Configuration

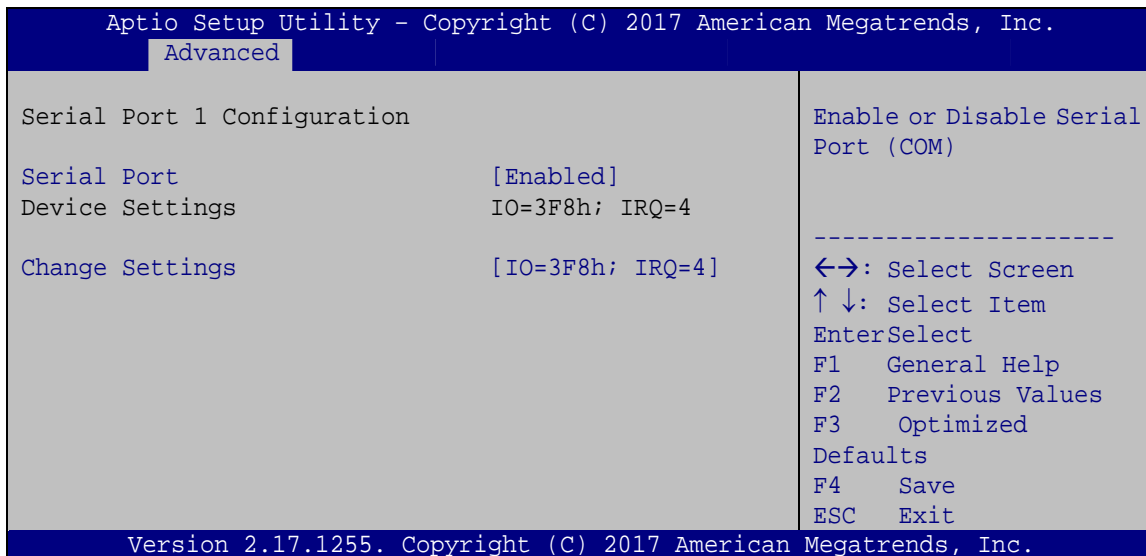
Set Parameters of Serial
Port 1 (COMA)
-----
<=>: Select Screen
↑↓: Select Item
EnterSelect
F1  General Help
F2  Previous Values
F3  Optimized
Defaults
F4  Save
ESC Exit

Version 2.17.1255. Copyright (C) 2017 American Megatrends, Inc.
  
```

**BIOS Menu 5: Super IO Configuration**

### 5.3.3.1 Serial Port n Configuration

Use the **Serial Port n Configuration** menu (**BIOS Menu 6**) to configure the serial port n.



#### BIOS Menu 6: Serial Port n Configuration

### 5.3.3.1.1 Serial Port 1 Configuration

#### → Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- **Disabled**                      Disable the serial port
- **Enabled      DEFAULT**      Enable the serial port

#### → Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- **IO=3F8h; IRQ=4      DEFAULT**      Serial Port I/O port address is 3F8h and the interrupt address is IRQ4
- **IO=3F8h; IRQ=3, 4, 11**                      Serial Port I/O port address is 3F8h and the interrupt address is IRQ3, 4, 11

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- IO=2F8h; IRQ=3, 4, 11      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 11
- IO=3E8h; IRQ=3, 4, 11      Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 11
- IO=2E8h; IRQ=3, 4, 11      Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 11

### 5.3.3.1.2 Serial Port 2 Configuration

#### → Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- Disabled      Disable the serial port
- Enabled      **DEFAULT**      Enable the serial port

#### → Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- IO=2F8h; IRQ=3      **DEFAULT**      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3
- IO=3F8h; IRQ=3, 4, 11      Serial Port I/O port address is 3F8h and the interrupt address is IRQ3, 4, 11
- IO=2F8h; IRQ=3, 4, 11      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 11
- IO=3E8h; IRQ=3, 4, 11      Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 11
- IO=2E8h; IRQ=3, 4, 11      Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 11

### 5.3.3.1.3 Serial Port 3 Configuration

➔ **Serial Port [Enabled]**

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled**                      Disable the serial port
- ➔ **Enabled      DEFAULT**      Enable the serial port

➔ **Change Settings [Auto]**

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- ➔ **IO=3E8h; IRQ=11      DEFAULT**      Serial Port I/O port address is 3E8h and the interrupt address is IRQ11
- ➔ **IO=2F8h; IRQ=3, 4, 11**                      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=3E8h; IRQ=3, 4, 11**                      Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=2E8h; IRQ=3, 4, 11**                      Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=2D0h; IRQ=3, 4, 11**                      Serial Port I/O port address is 2D0h and the interrupt address is IRQ3, 4, 11
- ➔ **IO=2E0h; IRQ=3, 4, 11**                      Serial Port I/O port address is 2E0h and the interrupt address is IRQ3, 4, 11





### 5.3.3.1.5 Serial Port 5 Configuration

#### → Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- **Disabled**                      Disable the serial port
- **Enabled**      **DEFAULT**      Enable the serial port

#### → Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- **IO=2D0h; IRQ=11**      **DEFAULT**      Serial Port I/O port address is 2D0h and the interrupt address is IRQ11
- **IO=2F8h; IRQ=3, 4, 11**      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 11
- **IO=3E8h; IRQ=3, 4, 11**      Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 11
- **IO=2E8h; IRQ=3, 4, 11**      Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 11
- **IO=2D0h; IRQ=3, 4, 11**      Serial Port I/O port address is 2D0h and the interrupt address is IRQ3, 4, 11
- **IO=2E0h; IRQ=3, 4, 11**      Serial Port I/O port address is 2E0h and the interrupt address is IRQ3, 4, 11

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## → Device Mode [RS232]

Use the **Device Mode** option to select the Serial Port 5 signaling mode.

- RS422                      Serial Port 5 signaling mode is RS-422
- RS232            **DEFAULT**      Serial Port 5 signaling mode is RS-232
- RS485                      Serial Port 5 signaling mode is RS-485

## 5.3.3.1.6 Serial Port 6 Configuration

## → Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- Disabled                      Disable the serial port
- Enabled            **DEFAULT**      Enable the serial port

## → Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- IO=2E0h; IRQ=11    **DEFAULT**      Serial Port I/O port address is 2E0h and the interrupt address is IRQ11
- IO=2F8h; IRQ=3, 4, 11                      Serial Port I/O port address is 2F8h and the interrupt address is IRQ3, 4, 11
- IO=3E8h; IRQ=3, 4, 11                      Serial Port I/O port address is 3E8h and the interrupt address is IRQ3, 4, 11
- IO=2E8h; IRQ=3, 4, 11                      Serial Port I/O port address is 2E8h and the interrupt address is IRQ3, 4, 11
- IO=2D0h; IRQ=3, 4, 11                      Serial Port I/O port address is 2D0h and the interrupt address is IRQ3, 4, 11

➔ IO=2E0h; IRQ=3, 4, 11

Serial Port I/O port address is 2E0h and the interrupt address is IRQ3, 4, 11

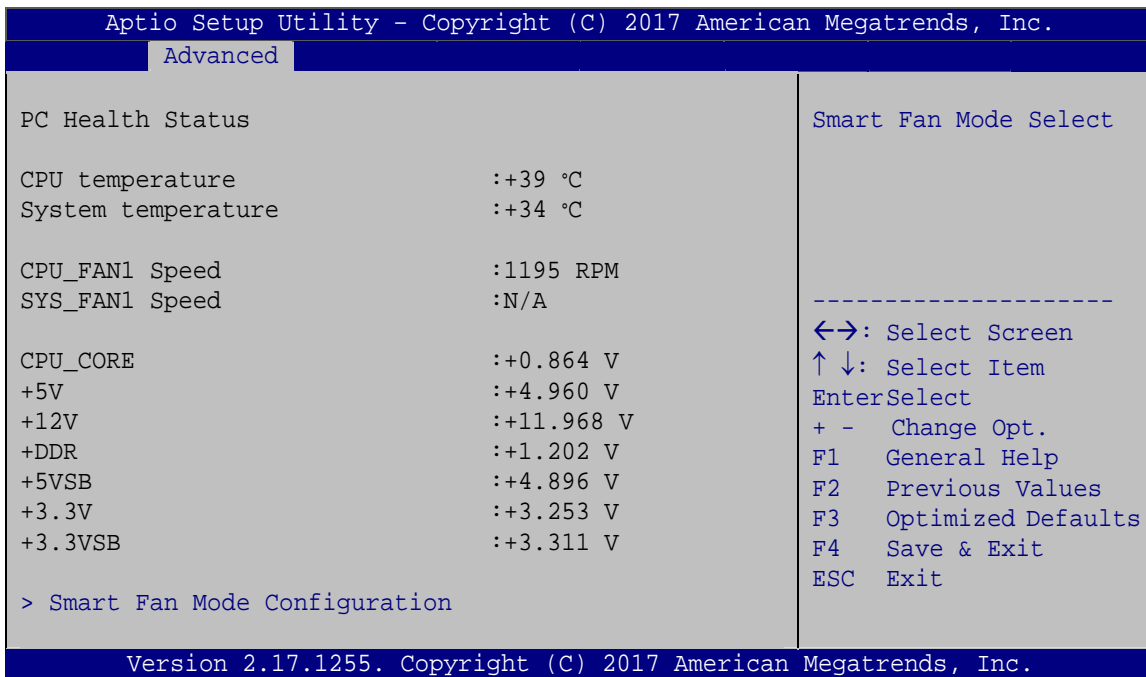
➔ **Device Mode [RS232]**

Use the **Device Mode** option to select the Serial Port 6 signaling mode.

- ➔ **RS422**                                      Serial Port 6 signaling mode is RS-422
- ➔ **RS232**                      **DEFAULT**      Serial Port 6 signaling mode is RS-232
- ➔ **RS485**                                      Serial Port 6 signaling mode is RS-485

**5.3.4 iWDD H/W Monitor**

The **iWDD H/W Monitor** menu (**BIOS Menu 7**) contains the fan configuration submenus and displays operating temperature, fan speeds and system voltages.



**BIOS Menu 7: iWDD H/W Monitor**

➔ **PC Health Status**

The following system parameters and values are shown. The system parameters that are monitored are:

## tKINO-ULT3 SBC

- System Temperatures:
  - CPU Temperature
  - System temperature
- Fan Speed:
  - CPU Fan Speed
  - System Fan Speed
- Voltages
  - CPU\_CORE
  - +5V
  - +12V
  - +DDR
  - +5VSB
  - +3.3V
  - +3.3VSB

### 5.3.4.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 8**) to configure fan temperature and speed settings.

```

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.
  Advanced
Smart Fan Mode Configuration
CPU_FAN1 Smart Fan Control      [Auto Mode]
Auto mode fan start temperature 50
Auto mode fan off temperature  40
Auto mode fan start PWM        30
Auto mode fan slope PWM        1
SYS_FAN1 Smart Fan Control      [Auto Mode]
Auto mode fan start temperature 50
Auto mode fan off temperature  40
Auto mode fan start PWM        30
Auto mode fan slope PWM        1
Smart Fan Mode Select
-----
<->: Select Screen
↑ ↓: Select Item
EnterSelect
+ - Change Opt.
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save & Exit
ESC Exit
Version 2.17.1255. Copyright (C) 2017 American Megatrends, Inc.
  
```

**BIOS Menu 8: Smart Fan Mode Configuration**



## tKINO-ULT3 SBC

The **Auto mode fan start temperature** option can only be set if the **CPU\_FAN1/SYS\_FAN1 Smart Fan Control** option is set to **Auto Mode**. If the system temperature is between **Start Temperature** and **Off Temperature**, the fan speed change to be **Start PWM**. To set a value, select the **Auto mode fan start temperature** option and enter a decimal number between 1 and 100.

### → Auto mode fan off temperature [40]

---



#### **WARNING:**

Setting this value too high may cause the fan to speed up only when the CPU is at a very high temperature and therefore cause the system to be damaged.

---

The **Auto mode fan off temperature** option can only be set if the **CPU\_FAN1/SYS\_FAN1 Smart Fan control** option is set to **Auto Mode**. If the system temperature is lower than **Auto mode fan off temperature**, the fan speed change to be lowest. To set a value, select the **Auto mode fan off temperature** option and enter a decimal number between 1 and 100.

### → Auto mode fan start PWM [30]

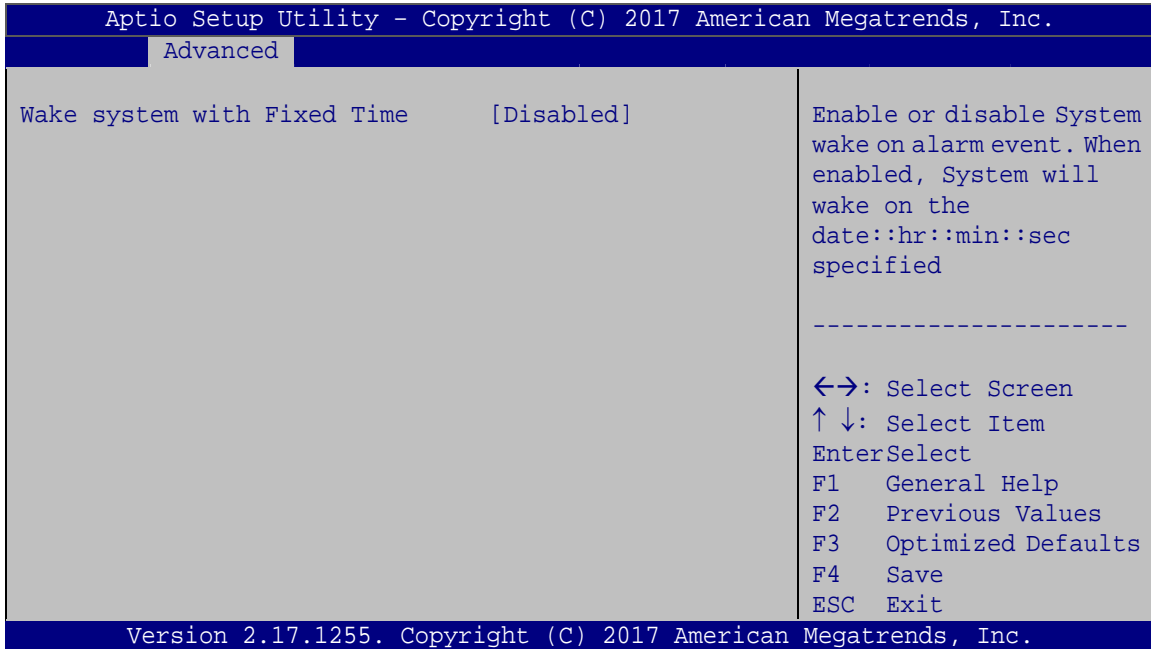
The **Auto mode fan start PWM** option can only be set if the **CPU\_FAN1/SYS\_FAN1 Smart Fan control** option is set to **Auto Mode**. Use the **Auto mode fan start PWM** option to set the PWM start value. To set a value, select the **Auto mode fan start PWM** option and enter a decimal number between 1 and 100.

### → Auto mode fan slope PWM [1]

The **Auto mode fan slope PWM** option can only be set if the **CPU\_FAN1/SYS\_FAN1 Smart Fan control** option is set to **Auto Mode**. Use the **Auto mode fan slope PWM** option to select the linear rate at which the PWM mode increases with respect to an increase in temperature. To set a value, select the **Auto mode fan slope PWM** option and enter a decimal number between 1 and 8.

### 5.3.5 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 9**) configures RTC wake event.



#### BIOS Menu 9: RTC Wake Settings

##### → Wake system with Fixed Time [Disabled]

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

- **Disabled**      **DEFAULT**      The real time clock (RTC) cannot generate a wake event
  
- **Enabled**                      If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected:
  - Wake up date
  - Wake up hour
  - Wake up minute

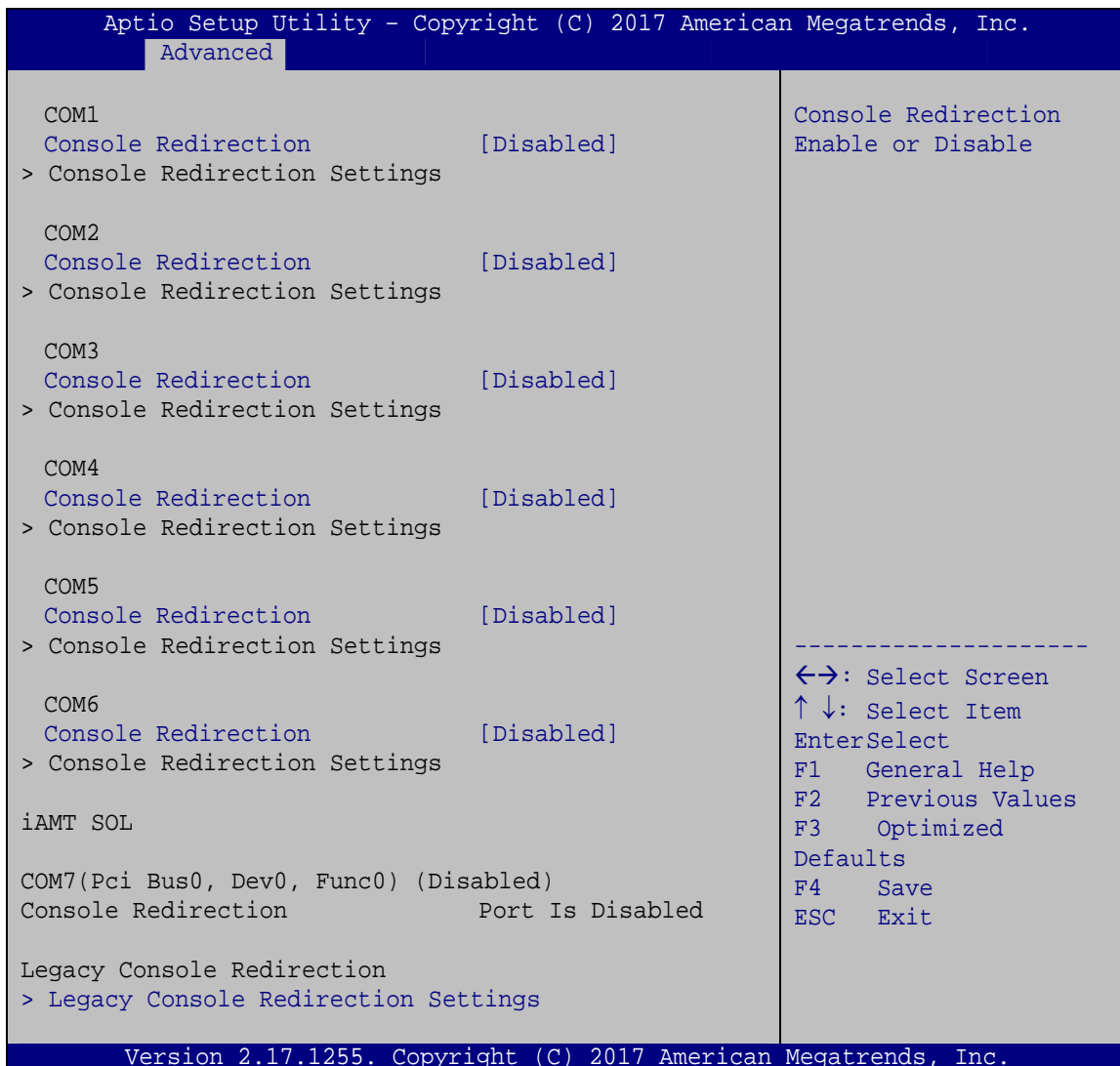


Wake up second

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

### 5.3.6 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 10**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



**BIOS Menu 10: Serial Port Console Redirection**

➔ **Console Redirection [Disabled]**

Use **Console Redirection** option to enable or disable the console redirection function.

- ➔ **Disabled**      **DEFAULT**      Disabled the console redirection function
- ➔ **Enabled**                      Enabled the console redirection function

**5.3.6.1 Legacy Console Redirection Settings**

The **Legacy Console Redirection Settings** menu (**BIOS Menu 11**) allows the legacy console redirection options to be configured.



**BIOS Menu 11: Legacy Console Redirection Settings**

➔ **Legacy Serial Redirection Port [COM1]**

Use the **Legacy Serial Redirection Port** option to specify a COM port to display redirection of legacy OS and legacy OPROM messages. The options include:

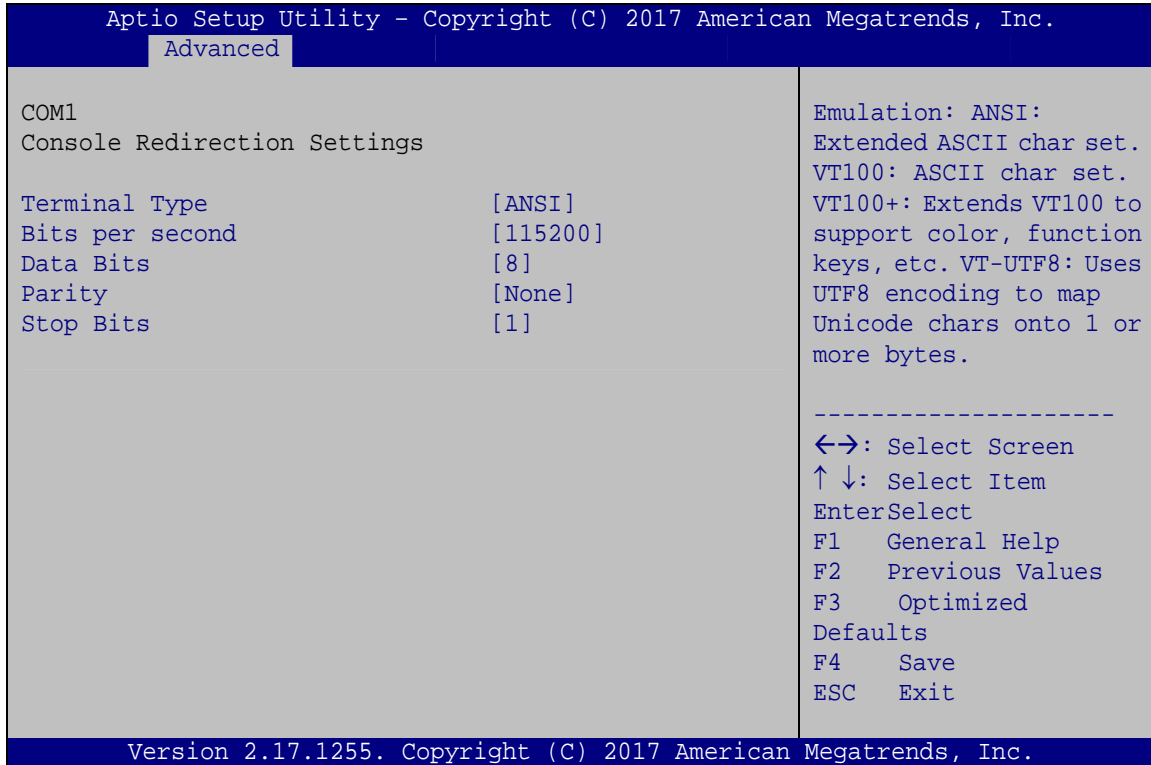
- COM1              **DEFAULT**
- COM2
- COM3
- COM4
- COM5

## tKINO-ULT3 SBC

- COM6
- COM7 (Pci Bus0, Dev0, Func0) (Disabled)

### 5.3.6.2 Console Redirection Settings

The **Console Redirection Settings** menu (**BIOS Menu 12**) allows the console redirection options to be configured. The option is active when Console Redirection option is enabled.



#### BIOS Menu 12: Console Redirection Settings

##### ➔ Terminal Type [ANSI]

Use the **Terminal Type** option to specify the remote terminal type.

- ➔ **VT100**                                      The target terminal type is VT100
- ➔ **VT100+**                                    The target terminal type is VT100+
- ➔ **VT-UTF8**                                    The target terminal type is VT-UTF8
- ➔ **ANSI**                                        **DEFAULT**                                    The target terminal type is ANSI

**→ Bits per second [115200]**

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

- **9600** Sets the serial port transmission speed at 9600.
- **19200** Sets the serial port transmission speed at 19200.
- **57600** Sets the serial port transmission speed at 57600.
- **115200** **DEFAULT** Sets the serial port transmission speed at 115200.

**→ Data Bits [8]**

Use the **Data Bits** option to specify the number of data bits.

- **7** Sets the data bits at 7.
- **8** **DEFAULT** Sets the data bits at 8.

**→ Parity [None]**

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- **None** **DEFAULT** No parity bit is sent with the data bits.
- **Even** The parity bit is 0 if the number of ones in the data bits is even.
- **Odd** The parity bit is 0 if the number of ones in the data bits is odd.
- **Mark** The parity bit is always 1. This option does not provide error detection.
- **Space** The parity bit is always 0. This option does not provide error detection.

## tKINO-ULT3 SBC

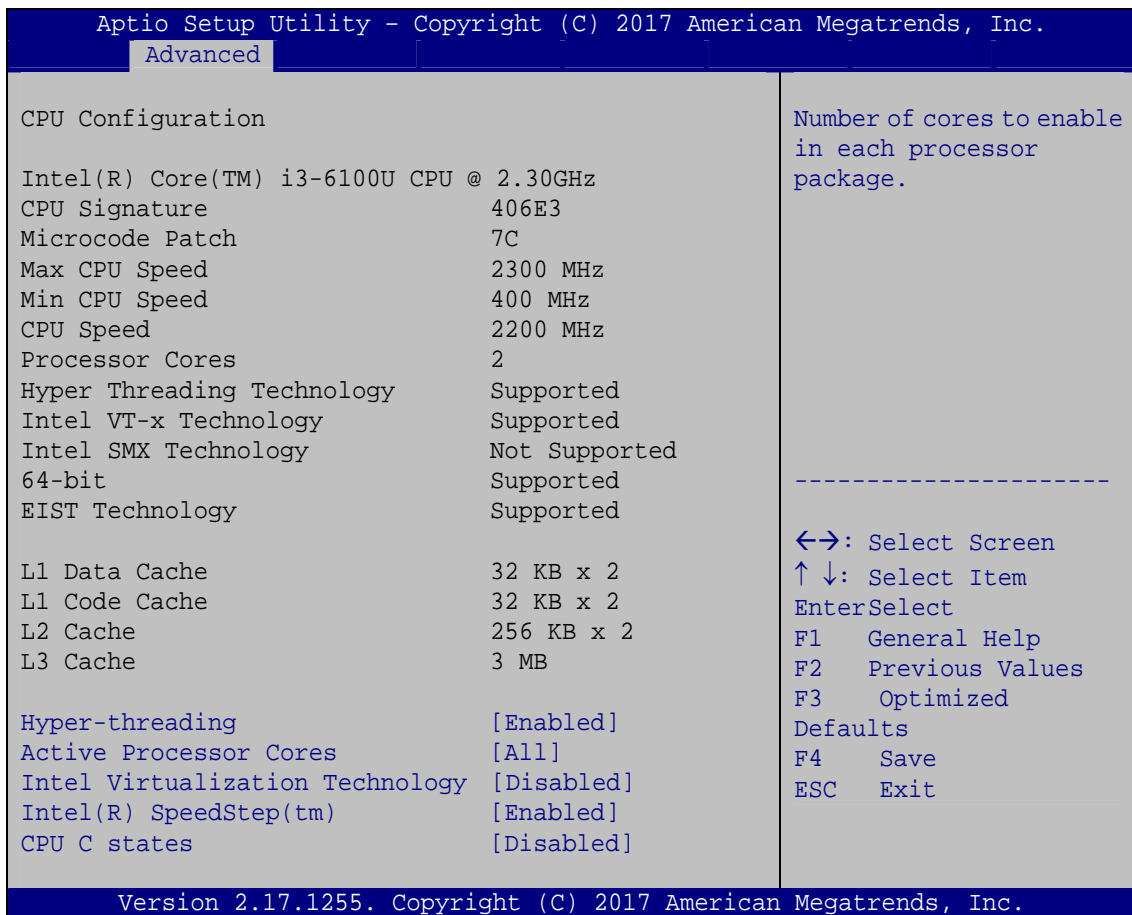
### → Stop Bits [1]

Use the **Stop Bits** option to specify the number of stop bits used to indicate the end of a serial data packet. Communication with slow devices may require more than 1 stop bit.

- 1                    **DEFAULT**        Sets the number of stop bits at 1.
- 2    Sets the number of stop bits at 2.

### 5.3.7 CPU Configuration

Use the **CPU Configuration** menu (**BIOS Menu 13**) to view detailed CPU specifications and configure the CPU.



Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.

Advanced

|  |               |  |
|--|---------------|--|
| CPU Configuration                        |               | Number of cores to enable in each processor package. |
| Intel(R) Core(TM) i3-6100U CPU @ 2.30GHz |               |  |
| CPU Signature                            | 406E3         |  |
| Microcode Patch                          | 7C            |  |
| Max CPU Speed                            | 2300 MHz      |  |
| Min CPU Speed                            | 400 MHz       |  |
| CPU Speed                                | 2200 MHz      |  |
| Processor Cores                          | 2             |  |
| Hyper Threading Technology               | Supported     |  |
| Intel VT-x Technology                    | Supported     |  |
| Intel SMX Technology                     | Not Supported |  |
| 64-bit                                   | Supported     |  |
| EIST Technology                          | Supported     |  |
| -----                                    |               |  |
| L1 Data Cache                            | 32 KB x 2     | ←→: Select Screen                                    |
| L1 Code Cache                            | 32 KB x 2     | ↑ ↓: Select Item                                     |
| L2 Cache                                 | 256 KB x 2    | EnterSelect  |
| L3 Cache                                 | 3 MB          | F1 General Help                                      |
| Hyper-threading                          | [Enabled]     | F2 Previous Values                                   |
| Active Processor Cores                   | [All]         | F3 Optimized   |
| Intel Virtualization Technology          | [Disabled]    | Defaults   |
| Intel(R) SpeedStep(tm)                   | [Enabled]     | F4 Save  |
| CPU C states                             | [Disabled]    | ESC Exit   |

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**BIOS Menu 13: CPU Configuration**

**→ Hyper-threading [Enabled]**

Use the **Hyper-threading** BIOS option to enable or disable the Intel Hyper-Threading Technology.

- **Disabled** Disables the Intel Hyper-Threading Technology.
- **Enabled** **DEFAULT** Enables the Intel Hyper-Threading Technology.

**→ Active Processor Cores [All]**

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

- **All** **DEFAULT** Enable all cores in the processor package.
- **1** Enable one core in the processor package.

**→ Intel® Virtualization Technology [Disabled]**

Use the **Intel® Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

- **Disabled** **DEFAULT** Disables Intel® Virtualization Technology.
- **Enabled** Enables Intel® Virtualization Technology.

**→ Intel® SpeedStep™ [Enabled]**

Use the **Intel® SpeedStep™** option to enable or disable the Intel® SpeedStep Technology.

- **Disabled** Disables the Intel® SpeedStep Technology.
- **Enabled** **DEFAULT** Enables the Intel® SpeedStep Technology.

## tKINO-ULT3 SBC

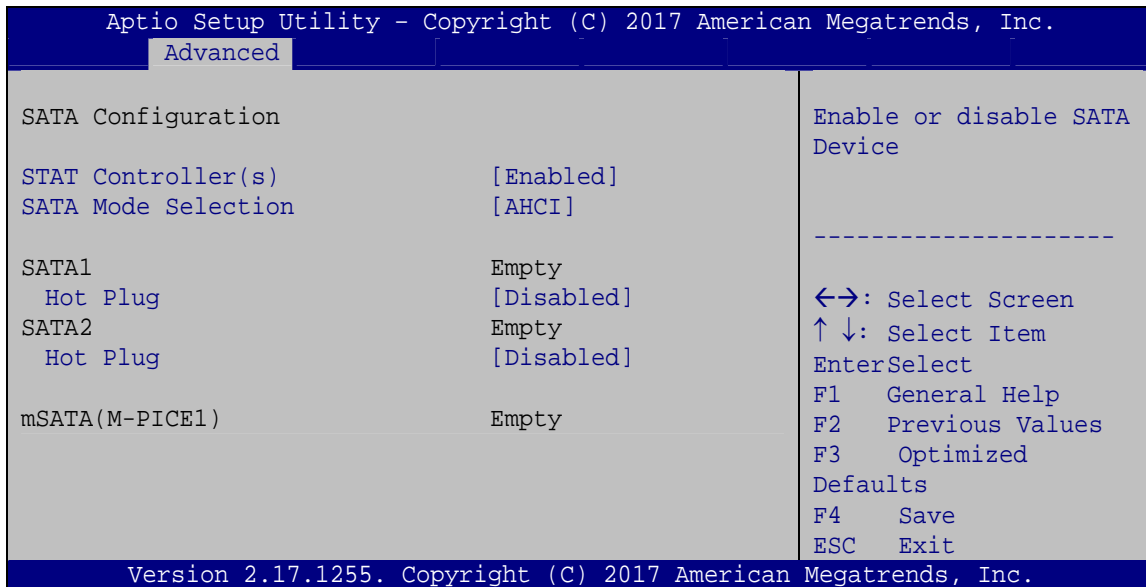
### → CPU C State [Disabled]

Use the **CPU C State** option to enable or disable CPU C state.

- **Disabled**    **DEFAULT**    Disables CPU C state.
- **Enabled**                      Enables CPU C state.

### 5.3.8 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 14**) to change and/or set the configuration of the SATA devices installed in the system.



#### BIOS Menu 14: SATA Configuration

### → STAT Controller(s) [Enabled]

Use the **STAT Controller(s)** option to enable or disable the SATA device.

- **Enabled**            **DEFAULT**    Enables the SATA device.
- **Disabled**                      Disables the SATA device.





## tKINO-ULT3 SBC

## 5.3.9 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 15**) to read USB configuration information and configure the USB settings.

```

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.
  Advanced
-----
USB Configuration
USB Controllers:
  1 XHCI
USB Devices:
  1 Keyboard
Legacy USB Support          [Enabled]

-----
<=>: Select Screen
↑↓: Select Item
Enter>Select
F1   General Help
F2   Previous Values
F3   Optimized
Defaults
F4   Save
ESC  Exit

Version 2.17.1255. Copyright (C) 2017 American Megatrends, Inc.

```

**BIOS Menu 15: USB Configuration**➔ **USB Devices**

The **USB Devices Enabled** field lists the USB devices that are enabled on the system

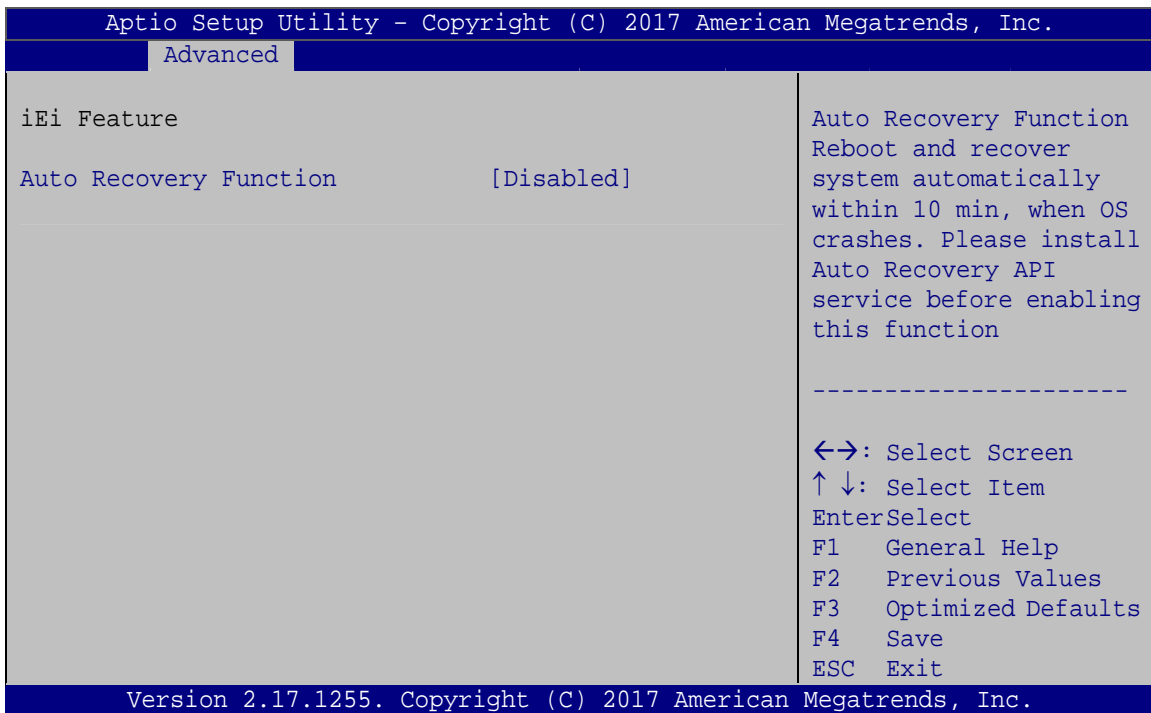
➔ **Legacy USB Support [Enabled]**

Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

- ➔ **Enabled**      **DEFAULT**      Legacy USB support enabled
- ➔ **Disabled**                      Legacy USB support disabled
- ➔ **Auto**                              Legacy USB support disabled if no USB devices are connected

### 5.3.10 IEI Feature

Use the **IEI Feature** menu (**BIOS Menu 16**) to configure One Key Recovery function.



#### BIOS Menu 16: IEI Feature

#### ➔ **Auto Recovery Function [Disabled]**

Use the **Auto Recovery Function** BIOS option to enable or disable the auto recovery function of the IEI One Key Recovery.

- ➔ **Disabled**      **DEFAULT**      Auto recovery function disabled
- ➔ **Enabled**                              Auto recovery function enabled

## 5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 17**) to configure the system chipset.

```

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.
Main   Advanced  Chipset  Security  Boot   Save & Exit
-----
> System Agent (SA) Configuration
> PCH-IO Configuration

System Agent (SA)
Parameters

-----
<=>: Select Screen
↑↓: Select Item
Enter>Select
+ - Change Opt.
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save & Exit
ESC Exit

Version 2.17.1255. Copyright (C) 2017 American Megatrends, Inc.
    
```

**BIOS Menu 17: Chipset**

### 5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 18**) to configure the System Agent (SA) parameters.

```

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.
Chipset
-----
VT-d                               [Disabled]          VT-d capability

> Graphics Configuration
> Memory Configuration

-----
<=>: Select Screen
↑↓: Select Item
Enter>Select
+ - Change Opt.
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save & Exit
ESC Exit

Version 2.17.1255. Copyright (C) 2017 American Megatrends, Inc.
    
```

**BIOS Menu 18: System Agent (SA) Configuration**

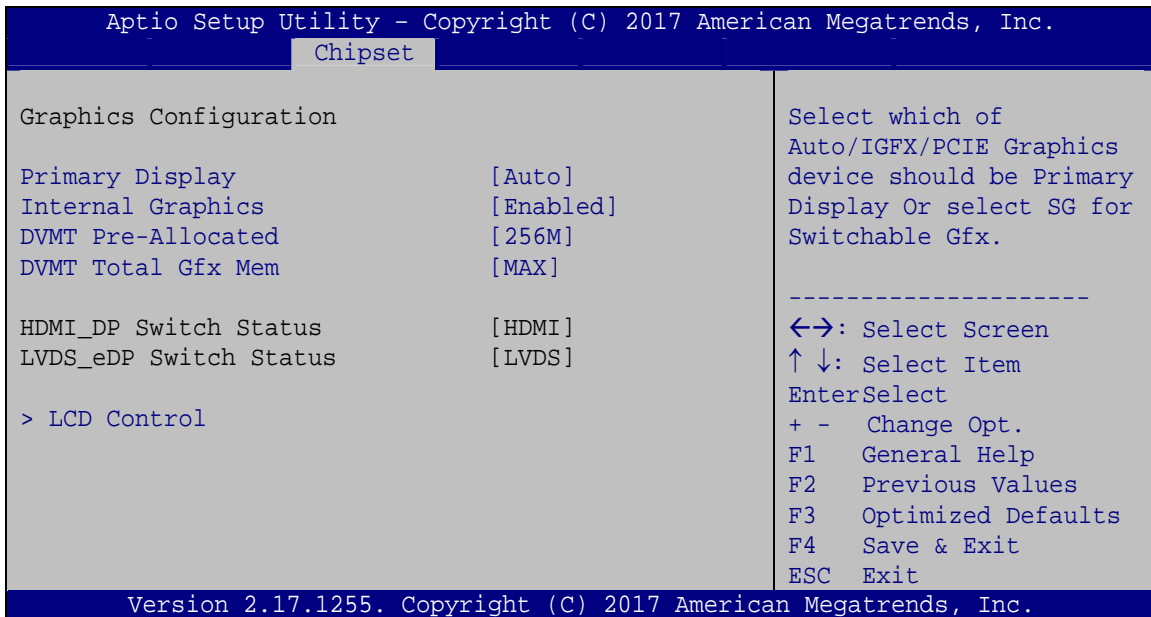
➔ **VT-d [Disabled]**

Use the **VT-d** option to enable or disable VT-d support.

- ➔ **Disabled**    **DEFAULT**    Disable VT-d support.
- ➔ **Enabled**                    Enable VT-d support.

### 5.4.1.1 Graphics Configuration

Use the **Graphics Configuration** menu (**BIOS Menu 19**) to configure the graphics settings.



#### BIOS Menu 19: Graphics Configuration

➔ **Primary Display [Auto]**

Use the **Primary Display** option to select the graphics controller used as the primary boot device. Configuration options are listed below:

- Auto                    **DEFAULT**
- IGFX
- PCIE

**tKINO-ULT3 SBC****→ Internal Graphics [Enabled]**

Use the **Internal Graphics** option to enable or disable the internal graphics device.

- Auto**                      The internal graphics device is automatically detected and enabled.
- Disabled**                Disable the internal graphics device.
- Enabled    DEFAULT**    Enable the internal graphics device. The following options/submenu appear with values that can be selected:

DVMT Pre-Allocated

DVMT Total Gfx Mem

LCD Control

**→ DVMT Pre-Allocated [256M]**

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- 32M
- 64M
- 128M
- 256M                      **DEFAULT**
- 512M

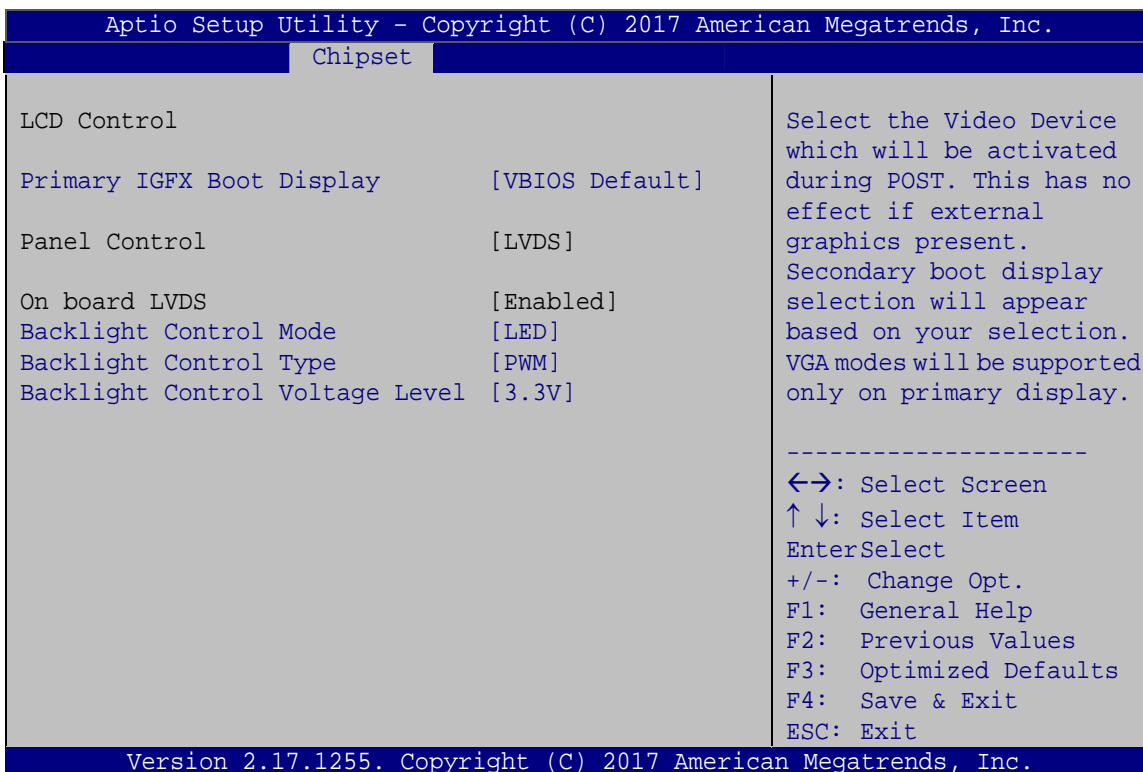
**→ DVMT Total Gfx Mem [MAX]**

Use the **DVMT Total Gfx Mem** option to select DVMT 5.0 total graphic memory size used by the internal graphics device. The following options are available:

- 128M
- 256M
- MAX                      **DEFAULT**

### 5.4.1.1.1 LCD Control

Use the **LCD Control** submenu (**BIOS Menu 20**) to select a display device which will be activated during POST.



#### BIOS Menu 20: LCD Control

##### → Primary IGFX Boot Display [VBIOS Default]

Use the **Primary IGFX Boot Display** option to select the display device used by the system when it boots.

- VBIOS Default **DEFAULT**
- HDMI1
- LVDS/eDP
- DP/HDMI2

##### → Backlight Control Mode [LED]

Use the **Backlight Control Mode** option to specify the backlight control mode. Configuration options are listed below.

## tKINO-ULT3 SBC

- LED                    **DEFAULT**
- CCFL

### → Backlight Control Type [PWM]

Use the **Backlight Control Type** option to specify the backlight control type. Configuration options are listed below.

- PWM                    **DEFAULT**
- DC

### → Backlight Control Voltage Level [3.3V]

Use the **Backlight Control Voltage Level** option to specify the backlight control voltage. Configuration options are listed below.

- 3.3V                    **DEFAULT**
- 5.0V

## 5.4.1.2 Memory Configuration

Use the **Memory Configuration** submenu (**BIOS Menu 21**) to display the memory information.

```

Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.
Chipset
-----
Memory Information
Total Memory          4096 MB
DIMM1                 4096 MB
DIMM2                 Not Present

-----
←→: Select Screen
↑ ↓: Select Item
EnterSelect
+ - Change Opt.
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save & Exit
ESC Exit

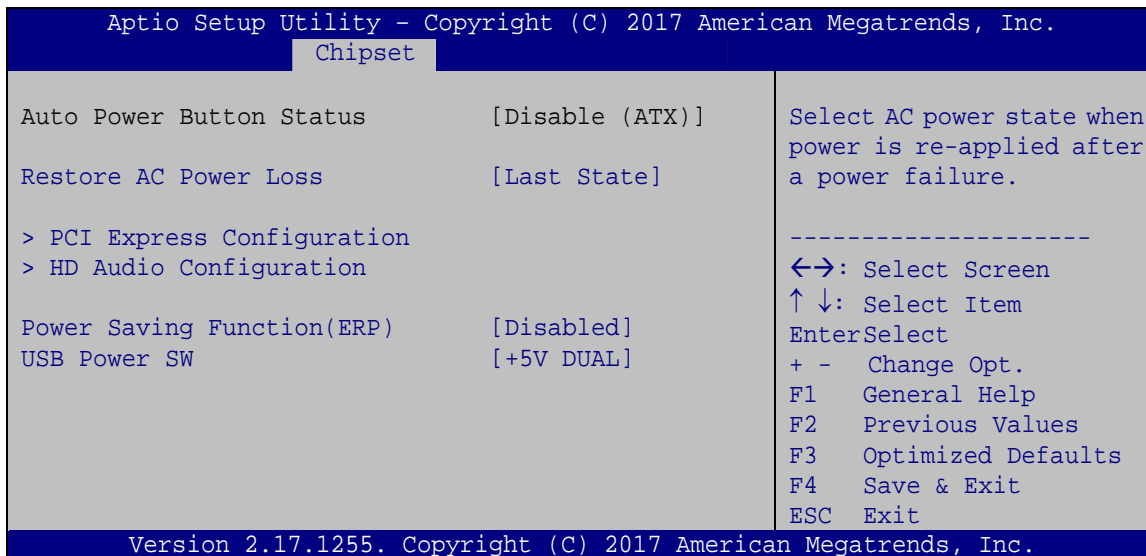
Version 2.17.1255. Copyright (C) 2017 American Megatrends, Inc.

```

**BIOS Menu 21: Memory Configuration**

## 5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 22**) to configure the PCH-IO chipset.



### BIOS Menu 22: PCH-IO Configuration

#### → Restore AC Power Loss [Last State]

Use the **Restore AC Power** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

- **Power Off**                      The system remains turned off
- **Power On**                        The system turns on
- **Last State    DEFAULT**        The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

#### → Power Saving Function(ERP) [Disabled]

Use the **Power Saving Function** BIOS option to enable or disable the power saving function.

- **Disabled    DEFAULT**        Power saving function is disabled.
- **Enabled**                        Power saving function is enabled. It will reduce power consumption when the system is off.



## tKINO-ULT3 SBC

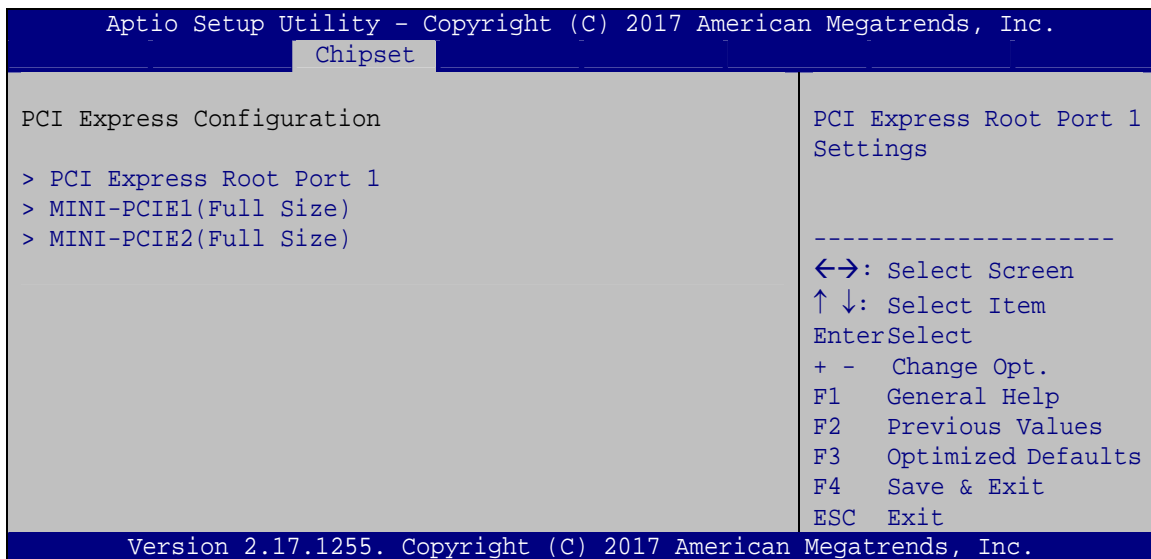
### → USB Power SW [+5V DUAL]

Use the **USB Power SW** BIOS option to configure the USB power source for all the external and internal USB connectors.

- **+5V            DEFAULT**    Set the USB power source to +5V dual  
**DUAL**
- **+5V**                            Set the USB power source to +5V

### 5.4.2.1 PCI Express Configuration

Use the **PCI Express Configuration** submenu (**BIOS Menu 23**) to configure the PCI Express slots.



#### BIOS Menu 23: PCI Express Configuration

The **PCI Express Root Port 1**, **MINI-PCIE1 (Full Size)** and **MINI-PCIE2 (Full Size)** submenus all contain the following options:

### → PCIe Speed [Auto]

Use the **PCIe Speed** option to configure the PCIe interface speed.

- Auto                    **DEFAULT**
- Gen 1
- Gen 2

- Gen 3

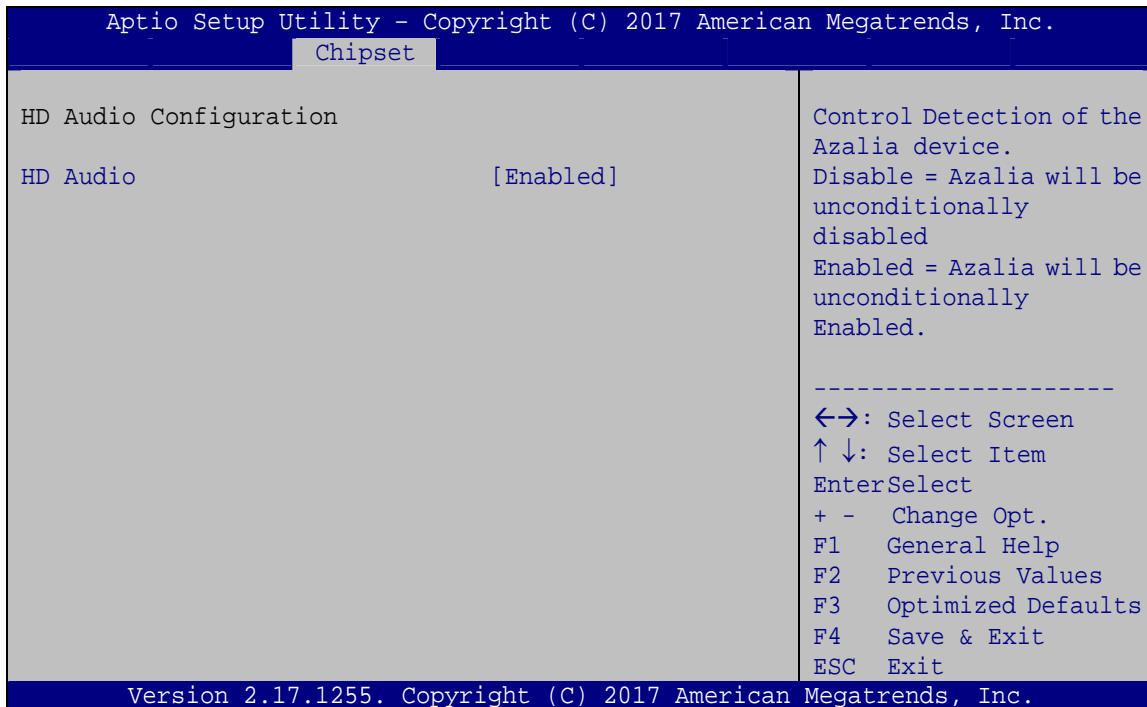
➔ **Detect Non-Compliance Device [Disabled]**

Use the **Detect Non-Compliance Device** option to enable or disable detecting if a non-compliance PCI Express device is connected to the PCI Express slot.

- ➔ **Disabled**                      **DEFAULT**      Disables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.
- ➔ **Enabled**                              Enables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.

**5.4.2.2 HD Audio Configuration**

Use the **HD Audio Configuration** submenu (**BIOS Menu 24**) to configure the High Definition Audio codec.



**BIOS Menu 24: HD Audio Configuration**

## tKINO-ULT3 SBC

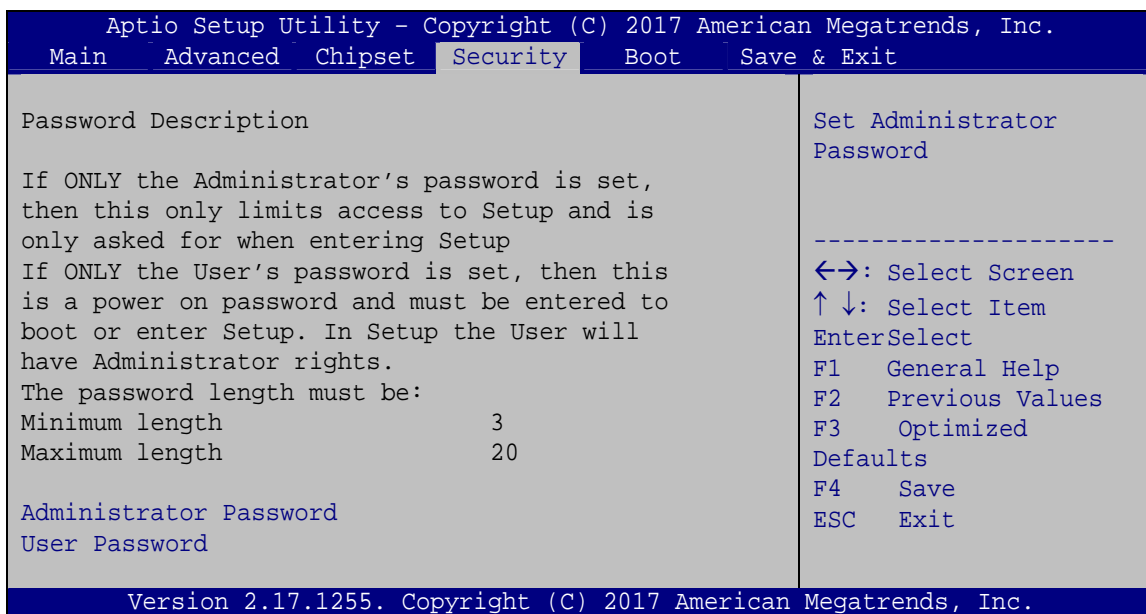
### → HD Audio [Enabled]

Use the **HD Audio** BIOS option to enable or disable the High Definition Audio controller.

- **Disabled**                      The High Definition Audio controller is disabled.
- **Enabled**      **DEFAULT**      The High Definition Audio controller is enabled.

## 5.5 Security

Use the **Security** menu (**BIOS Menu 25**) to set system and user passwords.



### BIOS Menu 25: Security

#### → Administrator Password

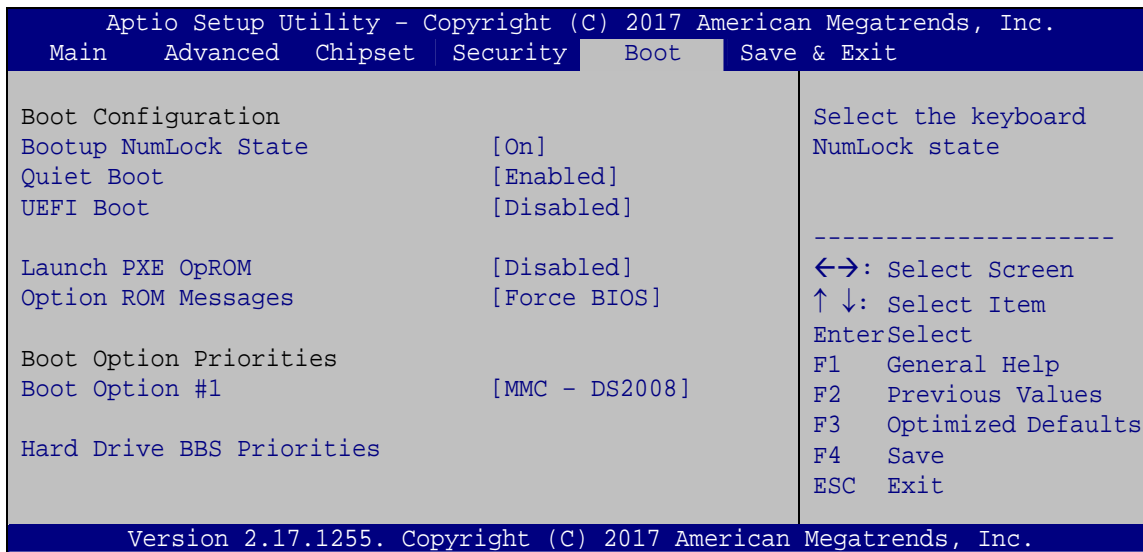
Use the **Administrator Password** to set or change a administrator password.

#### → User Password

Use the **User Password** to set or change a user password.

## 5.6 Boot

Use the **Boot** menu (**BIOS Menu 26**) to configure system boot options.



### BIOS Menu 26: Boot

#### → Bootup NumLock State [On]

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

- **On**                      **DEFAULT**                      Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.
  
- **Off**                                      Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

## tKINO-ULT3 SBC

→ **Quiet Boot [Enabled]**

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

- **Disabled** Normal POST messages displayed
- **Enabled** **DEFAULT** OEM Logo displayed instead of POST messages

→ **UEFI Boot [Disabled]**

Use the **UEFI Boot** option to enable or disable to boot from the UEFI devices.

- **Enabled** Boot from UEFI devices is enabled.
- **Disabled** **DEFAULT** Boot from UEFI devices is disabled.

→ **Launch PXE OpROM [Disabled]**

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

- **Disabled** **DEFAULT** Ignore all PXE Option ROMs
- **Enabled** Load PXE Option ROMs.

→ **Option ROM Messages [Force BIOS]**

Use the **Option ROM Messages** option to set the Option ROM display mode.

- **Force BIOS** **DEFAULT** Sets display mode to force BIOS.
- **Keep Current** Sets display mode to current.

→ **Boot Option Priority**

Use the **Boot Option Priority** function to set the system boot sequence from the available devices. The drive sequence also depends on the boot sequence in the individual device section.

## 5.7 Exit

Use the **Exit** menu (**BIOS Menu 27**) to load default BIOS values, optimal failsafe values and to save configuration changes.

```
Aptio Setup Utility - Copyright (C) 2017 American Megatrends, Inc.
Main   Advanced  Chipset  Security  Boot   Save & Exit
Save Changes and Reset
Discard Changes and Reset

Restore Defaults
Save as User Defaults
Restore User Defaults

Reset the system after
saving the changes.

-----
<->: Select Screen
↑ ↓: Select Item
Enter>Select
F1   General Help
F2   Previous Values
F3   Optimized
Defaults
F4   Save
ESC  Exit

Version 2.17.1255. Copyright (C) 2017 American Megatrends, Inc.
```

### BIOS Menu 27: Exit

#### → Save Changes and Reset

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and to exit the BIOS configuration setup program.

#### → Discard Changes and Reset

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

#### → Restore Defaults

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

## tKINO-ULT3 SBC

→ **Save as User Defaults**

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

→ **Restore User Defaults**

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Chapter

**6**

# Software Drivers

---



## tKINO-ULT3 SBC



### NOTE:

The content of the CD may vary throughout the life cycle of the product and is subject to change without prior notice. Visit the IEI website or contact technical support for the latest updates.

---

## 6.1 Software Installation

All the drivers for the tKINO-ULT3 are on the CD that came with the system. To install the drivers, please follow the steps below.

**Step 1:** Insert the CD into a CD drive connected to the system.

---



### NOTE:

If the installation program doesn't start automatically:  
Click "Start->My Computer->CD Drive->autorun.exe"

---

**Step 2:** The driver main menu appears.

**Step 3:** Click **tKINO-ULT3**.

**Step 4:** A new screen with a list of available drivers appears.

**Step 5:** Install all of the necessary drivers in the menu.

## 6.2 Available Software Drivers

All the drivers for the tKINO-ULT3 are on the utility CD that came with the system. The utility CD contains drivers for Windows 7, Windows 8.1 and Windows 10 operating systems. If the drivers are not installed automatically, please install the following drivers manually.

The following drivers can be installed on the **tKINO-ULT3**:

- Chipset
- VGA
- LAN
- Audio
- USB 3.0 (Windows 7/8.1 OS only)
- Kernel-Mode Driver Framework (Windows 7 OS only)
- ME (Intel® AMT)
- RST (Intel® Rapid Storage Technology)
- Intel® Serial IO (Windows 8.1/10 64-bit OS only)



### NOTE:

The Intel TXE requires that Microsoft's "Kernel-Mode Driver Framework (KMDF) version 1.11 update for Windows 7" must be installed first on Windows 7 OS. If the KMDF is not installed, either error 37 or error 28 may appear on the Intel TXE device in Device Manager.

Please find the KMDF version 1.11 update for Windows 7 in the TXE driver folder in the driver CD or click the following link to download it.

<http://www.microsoft.com/en-us/download/details.aspx?id=38423>

---

## 6.3 Installing Windows 7 from USB 3.0 Drives

Microsoft Windows 7 installation media does not include native driver support for USB 3.0, so during installation, a keyboard/mouse connected to a USB 3.0 port does not respond. The Windows 7 USB 3.0 Creator Utility automates the steps to update a Windows 7 installation image so that it contains USB 3.0 drivers. To install Windows 7 from a USB drive onto the tKINO-ULT3, please follow the steps described below.

- Step 1:** Create a USB flash drive installer. Use your Windows 7 DVD or ISO image to create a bootable USB flash drive. Instructions on how to do are found on [Microsoft's website](#).
- Step 2:** Download and unzip the [Windows 7 USB 3.0 Creator utility](#) to a temporary folder on the Admin system.
- Step 3:** Connect the USB device containing the Windows 7 image to the Admin system.
- Step 4:** Right-click the file "Installer\_Creator.exe" and select Run as administrator.
- Step 5:** Browse to the root of the USB drive.
- Step 6:** Click "Create Image" to begin the creation process.
- Step 7:** Wait for the process to finish. It can take up to 15 minutes.
- Step 8:** Using the updated installer, proceed with the Windows 7 installation as you normally would.

Appendix

**A**

# Regulatory Compliance

---

**DECLARATION OF CONFORMITY**

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

**FCC WARNING**

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

**B**

# Product Disposal

---

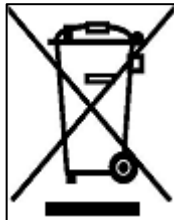
**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

---

- Outside the European Union – If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union – The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

# BIOS Menu Options

---



## tKINO-ULT3 SBC

|  |    |
|--|----|
| System Date [xx/xx/xx] .....                 | 76 |
| System Time [xx:xx:xx] .....                 | 76 |
| ACPI Sleep State [S3 (Suspend to RAM)] ..... | 77 |
| Intel AMT [Enabled] .....                    | 78 |
| Un-configure ME [Disabled] .....             | 78 |
| Serial Port [Enabled] .....                  | 80 |
| Change Settings [Auto] .....                 | 80 |
| Serial Port [Enabled] .....                  | 81 |
| Change Settings [Auto] .....                 | 81 |
| Serial Port [Enabled] .....                  | 82 |
| Change Settings [Auto] .....                 | 82 |
| Serial Port [Enabled] .....                  | 83 |
| Change Settings [Auto] .....                 | 83 |
| Serial Port [Enabled] .....                  | 84 |
| Change Settings [Auto] .....                 | 84 |
| Device Mode [RS232] .....                    | 85 |
| Serial Port [Enabled] .....                  | 85 |
| Change Settings [Auto] .....                 | 85 |
| Device Mode [RS232] .....                    | 86 |
| PC Health Status .....                       | 86 |
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| SYS_FAN1 Smart Fan Control [Auto Mode] ..... | 88 |
| Auto mode fan start temperature [50] .....   | 88 |
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| Auto mode fan start PWM [30] .....           | 89 |
| Auto mode fan slope PWM [1] .....            | 89 |
| Wake system with Fixed Time [Disabled] ..... | 90 |
| Console Redirection [Disabled] .....         | 92 |
| Legacy Serial Redirection Port [COM1] .....  | 92 |
| Terminal Type [ANSI] .....                   | 93 |
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| Data Bits [8] .....                          | 94 |
| Parity [None] .....                          | 94 |
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|   |     |
|---|-----|
| Hyper-threading [Enabled].....                    | 96  |
| Active Processor Cores [All] .....                | 96  |
| Intel® Virtualization Technology [Disabled] ..... | 96  |
| Intel® SpeedStep™ [Enabled] .....                 | 96  |
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| STAT Controller(s) [Enabled].....                 | 97  |
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| USB Devices .....                                 | 99  |
| Legacy USB Support [Enabled].....                 | 99  |
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| VT-d [Disabled].....                              | 102 |
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| Internal Graphics [Enabled].....                  | 103 |
| DVMT Pre-Allocated [256M] .....                   | 103 |
| DVMT Total Gfx Mem [MAX].....                     | 103 |
| Primary IGFX Boot Display [VBIOS Default] .....   | 104 |
| Backlight Control Mode [LED] .....                | 104 |
| Backlight Control Type [PWM] .....                | 105 |
| Backlight Control Voltage Level [3.3V].....       | 105 |
| Restore AC Power Loss [Last State] .....          | 106 |
| Power Saving Function(ERP) [Disabled].....        | 106 |
| USB Power SW [+5V DUAL].....                      | 107 |
| PCIe Speed [Auto].....                            | 107 |
| Detect Non-Compliance Device [Disabled] .....     | 108 |
| HD Audio [Enabled] .....                          | 109 |
| Administrator Password .....                      | 109 |
| User Password .....                               | 109 |
| Bootup NumLock State [On].....                    | 110 |
| Quiet Boot [Enabled] .....                        | 111 |
| UEFI Boot [Disabled] .....                        | 111 |
| Launch PXE OpROM [Disabled].....                  | 111 |
| Option ROM Messages [Force BIOS].....             | 111 |
| Boot Option Priority.....                         | 111 |
| Save Changes and Reset .....                      | 112 |

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|                                 |     |
|---------------------------------|-----|
| Discard Changes and Reset ..... | 112 |
| Restore Defaults .....          | 112 |
| Save as User Defaults .....     | 113 |
| Restore User Defaults .....     | 113 |

Appendix

**D**

# Terminology

---

## tKINO-ULT3 SBC

|          |  |
|----------|--|
| ACPI     | Advanced Configuration and Power Interface (ACPI) is an OS-directed configuration, power management, and thermal management interface.                                       |
| AHCI     | Advanced Host Controller Interface (AHCI) is a SATA Host controller register-level interface.  |
| ATA      | The Advanced Technology Attachment (ATA) interface connects storage devices including hard disks and CD-ROM drives to a computer.  |
| BIOS     | The Basic Input/Output System (BIOS) is firmware that is first run when the computer is turned on and can be configured by the end user                                      |
| CODEC    | The Compressor-Decompressor (CODEC) encodes and decodes digital audio data on the system.  |
| CMOS     | Complimentary metal-oxide-conductor is a type of integrated circuit used in chips like static RAM and microprocessors.   |
| COM      | COM is used to refer to serial ports. Serial ports offer serial communication to expansion devices. The serial port on a personal computer is usually a male DE-9 connector. |
| DDR      | Double Data Rate refers to a data bus transferring data on both the rising and falling edges of the clock signal.  |
| DIMM     | Dual Inline Memory Modules are a type of RAM that offer a 64-bit data bus and have separate electrical contacts on each side of the module.                                  |
| EHCI     | The Enhanced Host Controller Interface (EHCI) specification is a register-level interface description for USB 2.0 Host Controllers.  |
| GbE      | Gigabit Ethernet (GbE) is an Ethernet version that transfers data at 1.0 Gbps and complies with the IEEE 802.3-2005 standard.  |
| L1 Cache | The Level 1 Cache (L1 Cache) is a small memory cache built into the system processor.  |

|          |  |
|----------|--|
| L2 Cache | The Level 2 Cache (L2 Cache) is an external processor memory cache.  |
| LVDS     | Low-voltage differential signaling (LVDS) is a dual-wire, high-speed differential electrical signaling system commonly used to connect LCD displays to a computer.   |
| PCIe     | PCI Express (PCIe) is a communications bus that uses dual data lines for full-duplex (two-way) serial (point-to-point) communications between the SBC components and/or expansion cards and the SBC chipsets. Each line has a 2.5 Gbps data transmission rate and a 250 MBps sustained data transfer rate. |
| POST     | The Power-on Self Test (POST) is the pre-boot actions the system performs when the system is turned-on.  |
| RAM      | Random Access Memory (RAM) is a form of storage used in computer. RAM is volatile memory, so it loses its data when power is lost. RAM has very fast data transfer rates compared to other storage like hard drives.   |
| SATA     | Serial ATA (SATA) is a serial communications bus designed for data transfers between storage devices and the computer chipsets. The SATA bus has transfer speeds up to 1.5 Gbps and the SATA 3Gb/s bus has data transfer speeds of up to 3.0 Gbps.   |
| UART     | Universal Asynchronous Receiver-transmitter (UART) is responsible for asynchronous communications on the system and manages the system's serial communication (COM) ports.   |
| USB      | The Universal Serial Bus (USB) is an external bus standard for interfacing devices. USB 1.1 supports 12Mbps data transfer rates, while USB 2.0 supports 480Mbps data transfer rates.   |

Appendix

**E**

# Digital I/O Interface

---

The DIO connector on the tKINO-ULT3 is interfaced to GPIO ports on the Super I/O chipset. The DIO has both 8-bit digital inputs and 8-bit digital outputs. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.



**NOTE:**

For further information, please refer to the datasheet for the Super I/O chipset.

The BIOS interrupt call **INT 15H** controls the digital I/O.

**INT 15H:**

|                      |                                 |
|----------------------|---------------------------------|
| <b>AH – 6FH</b>      |                                 |
| <u>Sub-function:</u> |                                 |
| <b>AL – 8</b>        | : Set the digital port as INPUT |
| <b>AL</b>            | : Digital I/O input value       |

**Assembly Language Sample 1**

```

MOV     AX, 6F08H      ;setting the digital port as input
INT     15H           ;
    
```

**AL low byte = value**



|                      |                                  |
|----------------------|----------------------------------|
| <b>AH – 6FH</b>      |                                  |
| <u>Sub-function:</u> |                                  |
| <b>AL – 9</b>        | : Set the digital port as OUTPUT |
| <b>BL</b>            | : Digital I/O output value       |

### Assembly Language Sample 2

```
MOV    AX, 6F09H      ; setting the digital port as output  
MOV    BL, 09H        ; digital value is 09H  
INT    15H           ;
```

Digital Output is 1001b

Appendix

**F**

# Watchdog Timer

---

**NOTE:**

The following discussion applies to DOS. Contact IEI support or visit the IEI website for drivers for other operating systems.

The Watchdog Timer is a hardware-based timer that attempts to restart the system when it stops working. The system may stop working because of external EMI or software bugs. The Watchdog Timer ensures that standalone systems like ATMs will automatically attempt to restart in the case of system problems.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

| <b>AH – 6FH Sub-function:</b> |   |
|-------------------------------|---|
| AL – 2:                       | Sets the Watchdog Timer's period.   |
| BL:                           | Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup). |

**Table F-1: AH-6FH Sub-function**

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

**NOTE:**

The Watchdog Timer is activated through software. The software application that activates the Watchdog Timer must also deactivate it when closed. If the Watchdog Timer is not deactivated, the system will automatically restart after the Timer has finished its countdown.

**EXAMPLE PROGRAM:**

```
; INITIAL TIMER PERIOD COUNTER
```

```
;
```

```
W_LOOP:
```

```
;
```

```
MOV      AX, 6F02H      ;setting the time-out value  
MOV      BL, 30         ;time-out value is 48 seconds  
INT      15H
```

```
;
```

```
; ADD THE APPLICATION PROGRAM HERE
```

```
;
```

```
CMP      EXIT_AP, 1     ;is the application over?  
JNE      W_LOOP        ;No, restart the application
```

```
MOV      AX, 6F02H     ;disable Watchdog Timer  
MOV      BL, 0         ;  
INT      15H
```

```
;
```

```
; EXIT ;
```

Appendix

G

# Hazardous Materials Disclosure

---

The details provided in this appendix are to ensure that the product is compliant with the Peoples Republic of China (China) RoHS standards. The table below acknowledges the presences of small quantities of certain materials in the product, and is applicable to China RoHS only.

A label will be placed on each product to indicate the estimated “Environmentally Friendly Use Period” (EFUP). This is an estimate of the number of years that these substances would “not leak out or undergo abrupt change.” This product may contain replaceable sub-assemblies/components which have a shorter EFUP such as batteries and lamps. These components will be separately marked.

| Part Name   | Toxic or Hazardous Substances and Elements |              |              |                              |                                |                                       |
|---|--|--------------|--------------|------------------------------|--------------------------------|---------------------------------------|
|   | Lead (Pb)                                  | Mercury (Hg) | Cadmium (Cd) | Hexavalent Chromium (CR(VI)) | Polybrominated Biphenyls (PBB) | Polybrominated Diphenyl Ethers (PBDE) |
| Housing   | O  | O            | O            | O                            | O                              | O                                     |
| Display   | O  | O            | O            | O                            | O                              | O                                     |
| Printed Circuit Board   | O  | O            | O            | O                            | O                              | O                                     |
| Metal Fasteners   | O  | O            | O            | O                            | O                              | O                                     |
| Cable Assembly  | O  | O            | O            | O                            | O                              | O                                     |
| Fan Assembly  | O  | O            | O            | O                            | O                              | O                                     |
| Power Supply Assemblies   | O  | O            | O            | O                            | O                              | O                                     |
| Battery   | O  | O            | O            | O                            | O                              | O                                     |
| <p>O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).</p> <p>X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in SJ/T11363-2006 (now replaced by GB/T 26572-2011).</p> |  |              |              |                              |                                |                                       |

## tKINO-ULT3 SBC

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有“环境友好使用期限”的标签，此期限是估算这些物质“不会有泄漏或突变”的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

| 部件名称   | 有毒有害物质或元素 |           |           |                 |               |                 |
|--------|-----------|-----------|-----------|-----------------|---------------|-----------------|
|        | 铅<br>(Pb) | 汞<br>(Hg) | 镉<br>(Cd) | 六价铬<br>(CR(VI)) | 多溴联苯<br>(PBB) | 多溴二苯醚<br>(PBDE) |
| 壳体     | ○         | ○         | ○         | ○               | ○             | ○               |
| 显示     | ○         | ○         | ○         | ○               | ○             | ○               |
| 印刷电路板  | ○         | ○         | ○         | ○               | ○             | ○               |
| 金属螺帽   | ○         | ○         | ○         | ○               | ○             | ○               |
| 电缆组装   | ○         | ○         | ○         | ○               | ○             | ○               |
| 风扇组装   | ○         | ○         | ○         | ○               | ○             | ○               |
| 电力供应组装 | ○         | ○         | ○         | ○               | ○             | ○               |
| 电池     | ○         | ○         | ○         | ○               | ○             | ○               |

O: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11363-2006 (现由 GB/T 26572-2011 取代)标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11363-2006 (现由 GB/T 26572-2011 取代)标准规定的限量要求。